20. J. Lindenstrauss and L. Tzafriri, *Classical Banach spaces,* II, Springer-Verlag, Berlin and New York, 1979. MR 81c:46001
21. W. A. J. Luxemburg and A. C. Zaanen, *Riesz spaces,* I, North-Holland, Amsterdam, 1971. MR 58 #23483
22. R. J. Nagel, *Order in pure and applied functional analysis,* Trends in functional analysis and approximation theory (Acquafredda di Maratea, 1989), Univ. of Modena, Modena, 1991, pp. 87–1001.
23. H. Nakano, *Modern spectral theory,* Maruzen Co., Tokyo, 1950. MR 12, 419
24. ______, *Modulared semi-ordered linear spaces,* Maruzen Co., Tokyo, 1950. MR 12, 420
25. A. L. Peressini, *Ordered topological vector spaces,* Harper & Row, New York, 1967. MR 37 #3315
26. F. Riesz, *Sur la décomposition des opérations linéaires,* Atti Congr. Internaz. Mat. **3** (1930), 143–148.
27. ______, *Sur quelques notions fondamentales dans la théorie générale des opérations linéaires,* Ann. of Math. **41** (1940), 174–206. MR 1, 147
28. H. H. Schaefer, *Topological vector spaces,* Springer-Verlag, Berlin and New York, 1971. MR 33 #1689
29. ______, *Banach lattices and positive operators,* Springer-Verlag, Berlin and New York, 1974. MR 54 #11023
30. H.-U. Schwarz, *Banach lattices and operators,* Teubner-Texte Math., vol. 71, Teubner, Leipzig, 1984. MR 86h:46034
31. B. Z. Vulikh, *Introduction to the theory of partially ordered spaces,* Wolter-Hoordhoff, Groningen, Netherlands, 1967. MR 24 #A3494
32. Y. C. Wong and K. F. Ng, *Partially ordered topological vector spaces,* Clarendon Press, Oxford, 1973. MR 56 #12830
33. N. C. Yannelis, *The core of an economy with differential information,* Econom. Theory **1** (1991), 183–197.
34. A. C. Zaanen, *Riesz spaces,* II, North-Holland, Amsterdam and New York, 1983. MR 86b:46001

C. D. Aliprantis
Indiana University–Perdue University at Indianapolis

BULLETIN (New Series) OF THE
AMERICAN MATHEMATICAL SOCIETY
Volume 28, Number 1, January 1993

0273-0979/93 $1.00 + $.25 per page

Mathematical models in electrical circuits: theory and applications, By C. A. Marinov and P. Neittaanmäki. Kluwer Academic Publs., Dordrecht, 1991, 160 pp., $66.50. ISBN 0-7923-1155-8

With the advent of integrated circuits and the consequent highly miniaturized and densely packed semiconductor electronics, it has become impractical to design circuits by building prototypes and testing them to arrive at a satisfactory product. An unavoidable first step is to simulate proposed configurations with computer-aided analyses in order to obtain a promising initial design. Moreover, even that computational problem remains a severe one, for semiconductor chips are now being produced that contain several million transistors. As a result, current design simulations examine only small portions of those massive circuits and use fairly simplistic models of what are in fact quite complicated electrical networks. An additional complication is that such networks are inherently nonlinear, especially when used for digital technology, whereas the simplistic models are usually linearized. On the other hand, the abstract theory of nonlinear differential equations can, at least in principle, encompass massive models of physical systems. The book under review uses such mathematics to examine more realistic representations of integrated circuits. It is based upon a series of recent papers by the authors, which this book organizes into a unified exposition.

The history of nonlinear dynamic analyses of transistor circuitry extends back about three decades; some of the early efforts are [1, 4–9, 20–23]. Many of those and more recent works concern qualitative properties such as existence, uniqueness, and stability of solutions, although considerable effort has also been expended toward computational problems. The present book is a timely contribution to that body of research and extends it in several directions. A notable advance is the allowance of more general kinds of nonlinearities. Prior works assumed continuous differentiability or piecewise linearity for the resistive part of the circuitry, whereas Marinov and Neittaanmäki merely allow continuity with piecewise-continuous differentiability for those resistances.

Another novel contribution is their analysis of delay time for transients. The estimation of delay time has become a pressing issue in the design of switching circuits because, with current levels of miniaturization in semiconductor electronics, the principle constraints on clock speeds for computer circuitry arise from the delays among interconnection lines. During the past decade considerable effort has been devoted to obtaining rapid and yet acceptably accurate estimations of delay times. A sampling of such research during the past decade is [2, 3, 10, 12–19, 24, 25, 27, 28]. Marinov and Neittaanmäki propose a significant innovation in this research area. Rather than estimating the delay times along particular input-to-output paths, they construct a global delay-time criterion that applies simultaneously to the settling of all the voltages in the circuit. This allows the setting of clock frequency without having to examine many input-to-output paths individually. Furthermore, they use distributed-line models for the interconnections, these being more accurate than lumped models. In doing all this, however, they resort to a linear analysis. Moreover, the feasibility of their delay-time measure for practical circuits is questionable, for it appears that computational complexity expands exponentially with the number of transmission lines. Nonetheless, their results may lead to some important design tools.

A more detailed discussion of the book now follows. The first half of it is devoted to the analysis of lumped circuits with bipolar transistors, diodes, resistors, capacitors, and inductances, all of which may have nonlinear characteristics. That analysis is based upon the theory of ordinary differential equations in a Banach space X, such as the nonlinear initial-value problem: $du/dt = A(t)u(t)$, $u(0) \in X$, where u maps the real positive line R_+ into X and A maps R_+ into the space of dissipative operators with domains and ranges in X. The point is that various design problems for bipolar transistor circuits can be formulated in these abstract terms, hence, making them amenable to powerful techniques from nonlinear functional analysis. Marinov and Niettaanmäki exploit this theory on abstract differential equations to obtain some new applications concerning both the dynamic and steady-state DC behavior of electronic circuits. A knowledge of nonlinear functional analysis is required for a comprehension of their exposition of some primarily standard theory, as also is a familiarity with semigroups of linear dissipative operators, for that too is used in the second half of the book as well.

Qualitative properties of the said bipolar transistor circuits are then examined, such as the existence and uniqueness of solutions, their boundedness and stability, and their asymptotic behavior as time tends to infinity. A notable generalization in the book is the modeling of the resistive part of the network with nonlinear, continuous, and piecewise-continuously-differentiable characteristics, instead of the linear or piecewise-linear continuous characteristics of prior works. Also, the other elements are modeled by continuous piecewise-linear characteristics rather than the continuously differentiable characteristics of prior models. All this leads to a quite general, albeit complicated, model of the transistor network. Both strong solutions and, under a strengthening of the hypotheses, classical solutions are obtained. Moreover, different initial conditions lead asymptotically to the same unique DC operating state. Thus, the considered electrical network—although nonlinear—does not admit multiple operating points. The continuity of the final state with respect to variations in biasing is also shown.

Another generalization this book offers is an analysis of infinite electrical networks consisting of finitely many voltage sources and bipolar transistors but infinitely many resistors and capacitors. This is of physical interest because certain distributed-parameter transmission-line configurations, when discretized by lumped parameters, become infinite lumped networks [11]. Although there is presently a fairly substantial body of knowledge concerning purely resistive infinite networks [26], not much is known about the transient behavior of nonlinear networks with reactances and active elements. Dolezal's work [7, 8] is the notable achievement in this area, but his results are quite abstract and difficult to apply to VLSI circuits. Marinov and Neittaanmäki adopt a more specific and restricted approach and achieve thereby more explicit results. They construct one of the very few analyses in this difficult area of research.

The second half of the book abandons nonlinear analysis in order to examine the dynamic behavior of switching circuits wherein the transistors are for the most part field-effect transistors rather than bipolar transistors. In any case, all transistors are now modeled by linear resistors, and the network's transients are examined between consecutive switching times. A primary objective is the estimation of a global measure of all the delays in signaling; that measure is taken to be the time required for all the transient voltages to traverse a specified fraction of their total variations. Since the principal hindrance to small delay times under current integrated-circuit miniaturization has become the propagations along the interconnections lines, it is important to model those lines more accurately with distributed parameters rather than with lumped elements. This leads to a "mixed network" consisting both of distributed parameters for those interconnection lines and also with lumped elements for the transistors, resistors, and capacitors. Actually the inductances of the lines are ignored, with the result that those lines are analyzed as diffusion channels rather than as wave channels; this restricts the applicability of the analysis with regard to the higher frequencies. Nonetheless, this mixed model is an important improvement over the lumped and overly simplistic models of many prior works.

Here, too, Marinov and Neittaanmäki have set up a model of wide generality for all kinds of switching circuits. Its mathematical structure is a set of parabolic partial differential equations representing the interconnection lines, with boundary conditions at the terminals of those lines representing their coupling with the lumped parameters—and also with initial conditions along the lines. All this comprises a rather complicated Cauchy problem, and its solution involves some Schwartz distributions because the initial conditions are not required to be differentiable everywhere. Correspondingly, the final steady state is governed by a set of linear ordinary differential equations obtained from the prior Cauchy problem by deleting all time derivatives. Once again, existence and uniqueness results are derived for both the dynamic and steady-state problems. The continuity of the solutions with respect to variations in biasing and in initial conditions is established. It is also shown that the transients settle to the same DC values, whatever be the initial conditions.

As for the estimation of a global delay-time measure, it is assumed that all transistors are switched just before the initial conditions are applied and maintain constant resistance values during the transient period. Thus, transient behavior within the transistors is ignored. The global delay-time criterion that Marinov and Neittaanmäki propose is the time it takes for the slowest transient to achieve a given fraction of its total variation. Since no inductances are considered and since all capacitors are connected to a common ground, all transients are monotonic. This simplifies the determination of a unique value for that criterion. The fact that their delay-time measure applies to all transients taken simultaneously is a major advantage of their formulation. Moreover, they derive an upper bound on that measure, which can be computed directly from the element values without having to solve the aforementioned Cauchy problem. One might expect that some payment will be extracted for such generality; it is in computational complexity—the computations expand exponentially with the number of transmission lines. The three examples they present involve only two or four transmission lines and about 10 to 15 other parameters. For these examples the upper bounds are not unreasonably loose, being roughly two to four times the actual delay time measures, the latter being computed through some standard numerical techniques. All this may prove to be quite important whenever computations remain manageable.

In summary, this book addresses some currently critical problems in electrical engineering, but it demands a knowledge of modern theories of differential equations. It will probably be of greatest interest to mathematicians seeking applications to current technologies, but here too some knowledge of electronic devices and circuits will render the book more accessible. The powerful methods of functional analysis can help to solve some incipient and complicated problems in integrated-circuits design. This book may be a harbinger of much more.

References

1. R. K. Brayton and W. L. Miranker, *A stability theory for nonlinear mixed initial boundary value problems*, Arch. Rational Mech. Anal. **17** (1964), 358–376.
2. P. K. Chan and K. Karplus, *Computing signal delay in general RC networks by tree/link partitioning*, IEEE Trans. Comput. Aided Design **9** (1990), 898–902.
3. P. K. Chan and M. D. F. Schlag, *Bounds on signal delay in RC mesh networks*, IEEE Trans. Comput. Aided Design **8** (1989), 581–589.
4. L. O. Chua and D. N. Green, *A qualitative analysis of the behavior of dynamic nonlinear networks—stability of autonomous networks*, IEEE Trans. Circuits and Systems **23** (1976), 355–379.

5. ______, *A qualitative analysis of the behavior of dynamic nonlinear networks: steady-state solutions of nonautonomous networks*, IEEE Trans. Circuits and Systems **23** (1976), 530–550.
6. C. A. Desoer and J. Katznelson, *Nonlinear RLC networks*, Bell Syst. Tech. J. **44** (1965), 161–198.
7. V. Dolezal, *Nonlinear networks*, Elsevier Sci. Publ. Co., New York, 1977.
8. ______, *Monotone operators and applications in control and network theory*, Elsevier Sci. Publ. Co., New York, 1979.
9. T. Fujisawa and E. S. Kuh, *Some results on existence and uniqueness of solutions of nonlinear networks*, IEEE Trans. Circuit Theory **18** (1971), 389–394.
10. D. S. Gao, A. T. Yang, and S. M. Kang, *Modelling and simulation of interconnection delays and crosstalks in high-speed integrated circuits*, IEEE Trans. Circuits and Systems **37** (1990), 1–9.
11. M. S. Ghausi and J. J. Kelly, *Introduction to distributed parameter networks*, Holt, Rinehart, and Winston, New York, 1968.
12. R. O. Grondin, W. Porod, and D. K. Ferry, *Delay time and signal propagation in large-scale integrated circuits*, IEEE J. Solid-State Circuits **19** (1984), 262–263.
13. M. G. Harbour and J. M. Drake, *Calculation of signal delay in integrated interconnections*, IEEE Trans. Circuits and Systems **36** (1989), 272–276.
14. T. M. Lin and C. A. Mead, *Signal delay in general RC networks*, IEEE Trans. Comput. Aided Design **3** (1984), 331–349.
15. J. K. Ousterhout, *A switch-level timing verifier for digital MOS VLSI*, IEEE Trans. Comput. Aided Design **4** (1985), 336–349.
16. M. Passlack, M. Uhle, and H. Elschner, *Analysis of propagation delays in high-speed VLSI circuits using a distributed line model*, IEEE Trans. Comput. Aided Design **9** (1990), 821–826.
17. L. T. Pillage and R. A. Rohrer, *Asymptotic waveform evaluation for timing analysis*, IEEE Trans. Comput. Aided Design **9** (1990), 352–366.
18. J. Rubinstein, P. Penfield, Jr., and M. A. Horowitz, *Signal delay in RC tree networks*, IEEE Trans. Comput. Aided Design **2** (1983), 202–211.
19. T. Sakarai, *Approximation of wiring delay in MOSFET LSI*, IEEE J. Solid-State Circuits **18** (1983), 418–426.
20. I. W. Sandberg, *Some theorems on the dynamic response of transistor networks*, Bell Syst. Tech. J. **48** (1969), 35–54.
21. ______, *Theorems on the analysis of nonlinear transistor networks*, Bell Syst. Tech. J. **49** (1970), 95–114.
22. A. N. Willson, Jr.,, *On the solution of equations for nonlinear resistive networks*, Bell Syst. Tech. J. **47** (1968), 1755–1773.
23. ______, *New theorems on the equations of nonlinear dc transistor networks*, Bell Syst. Tech. J. **49** (1970), 1713–1738.
24. J. L. Wyatt, Jr., *Monotone sensitivity of nonlinear RC transmission lines with application to timing analysis of digital MOS integrated circuits*, IEEE Trans. Circuits and Systems **32** (1985), 28–33.
25. Q. Yu and O. Wing, *Waveform bounds on nonlinear RC trees*, Proc. 1984 Internat. Sympos. on Circuits and Systems, Montreal, 1984.
26. A. H. Zemanian, *Infinite electrical networks*, Cambridge Univ. Press, New York, 1991.
27. C. A. Zukowski, *The bounding approach to VLSI circuit simulation*, Kluwer Academic Press, Dordrecht, 1986.
28. J. M. Zurada and T. Liu, *Equivalent dominant pole approximation of capacitively loaded VLSI interconnection*, IEEE Trans. Circuits and Systems **34** (1987), 205–207.

A. H. ZEMANIAN
STATE UNIVERSITY OF NEW YORK AT STONY BROOK
E-mail address: zeman@sbee.sunysb.edu