AUTOMATIC COMPUTING MACHINERY

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TECHNICAL DEVELOPMENTS

The BARK, A Swedish General Purpose Relay Computer

Introduction.—In December 1948 The Swedish Board for Computing Machinery decided to build a relay digital computer for which plans and cost estimates had been drawn up by DR. CONNY PALM. Design work started almost immediately under the direction of Dr. Palm. The machine was completed in February 1950 and, after a testing period, was inaugurated on April 28, 1950. The machine is called BARK, standing for "Binär Automatisk Relä Kalkylator." The main characteristics of the computer are listed below.

Numbers are represented by absolute value and sign in the form $2^p \cdot q$, where p is a 6-digit binary number with algebraic sign and q is a 24-digit binary fraction with algebraic sign. Thus, 32 binary characters are required for the representation of one number. In the decimal system this corresponds to a range between 10^{-19} and 10^{+19} with a precision of slightly better than seven decimal digits.

In the number representation, q plus the sign is referred to as the "numerical part" of the number, while the remaining places are called the "exponential part." Similarly, in the following, the 25 places of a register which store the digits and sign of the fraction q will be referred to as the "numerical part" of the register, while the remaining places will be called the "exponential part." Within each part we use the terms "first" or "left-(most)" to designate the most significant positions or digits, while "last" or "right(most)" describe the least significant positions.

Storage and Arithmetic Circuits.—The storage consists of 50 relay registers and 100 constant registers, each storing 32 binary characters. In the near future the memory capacity will be increased to 100 relay registers and 200 constant registers. The original design enables this enlargement to be made without difficulty. The constant registers are set manually by means of one 4-position switch for the signs and ten 8-position switches, each one taking care of three binary digits; conversion to binary form is thus necessary before a number is put in a constant register.

Within the machine numbers are transferred along three number transfer busses, each of which contains 32 wires or digit channels. Voltage on a digit channel represents the digit one or a plus-sign; no voltage represents the digit zero or a minus-sign. The A- and the B-busses transmit numbers from the storage to the arithmetic circuits, and the C-bus transmits numbers in the opposite direction.

The arithmetic circuits carry out transfer, addition, and multiplication with arbitrary signs for the numbers involved.

Transfers include transfer with opposite sign, transfer of absolute value and negative absolute value, and logical addition (i.e., the transfer of the logical sum of two numbers). Technically a transfer is accomplished when corresponding digit channels in each of the three busses are interconnected. From this it follows that the ordinary transfer is a special case of logical addition, where one of the two numbers consists of zeros (or minus signs) on all wires.

The adder shifts the number having the smaller exponent to its proper position and then forms the arithmetically correct sum or difference of the two numbers. The shifted number is not rounded off. If the sum of the numerical parts of the two numbers should exceed one, the result is shifted one position to the right and its exponent increased by one. In this case the
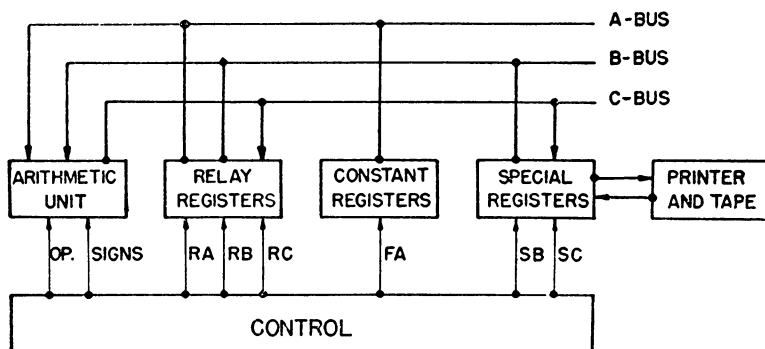

Fig. 1.

result is rounded off before the shift is made. If, on the other hand, the sum or difference should be less than one-half, the result is not shifted. The first digit of the result is therefore not necessarily a one.

The adder contains 232 relays. Addition is carried out in five successive steps. First, exponents and signs are compared. Second, the difference is taken between the two exponents and simultaneously the number to be shifted is selected. Third, the shift is carried out and the number not shifted is inverted, if necessary. (Nines complements are used.) Fourth, the addition of the two numerical parts is carried out. Fifth, the sum is shifted one position to the right, or inverted, or left unchanged, whichever the case may be. Simultaneously the exponent of the result is increased by one if the sum was shifted, and the sign of the numerical part is formed. A chain of slower relays controls the timing, so that no step is started before the previous one is completed.

Multiplication is carried out in the following way: The two numbers coming in are first "normalized," that is, shifted to the left until the first binary one occupies the leftmost position. [This operation is called a "zeroshift" in the report on the BTL Relay Computers (*MTAC*, v. 3, p. 1–13; 69–84).] The exponents are modified accordingly. In the rest of the multiplication the numerical parts of multiplier (MR) and multiplicand (MD) are treated as 8-digit numbers in the octal number system, since a group of three binary digits forms one octal digit. Multiples of MD with the integers 1, 2, ···, 7 are formed and selected simultaneously by the eight octal digits

of MR. The multiples are added together in seven adders in such a way that only 30 binary digits, or ten octal digits, are retained for the final result. In order to compensate for the digits that are dropped an octal three is added in the tenth octal position. When the whole product is formed, a binary one is added into the twenty-fifth binary position and the 24 first digits retained. The multiplier thus delivers a correctly rounded 24-digit product, where, however, the first digit may be a zero. No provision has been made for computation with double accuracy. Such computation can still be done by a coded sequence of instructions but turns out to be extremely cumbersome and is therefore in most cases impracticable. Altogether the multiplier contains 923 relays.

Normalization of a single number can also be carried out. One of the two normalizing circuits in the multiplier is then connected to the A- and the C-bus. The rest of the multiplier is not affected by this operation.

Other elementary operations where only one number is involved at a time are handled by special circuits. These operations are:

1. Transfer of an exponent to the last six places of the numerical part of a register
2. Transfer of the last six digits of a numerical part into the exponential part of a register
3. Transfer of the numerical part only
4. Transfer of the fractional part of a number (for example, in 23.67 the fractional part is 0.67)
5. Shift one step to the left (or to the right) of the numerical part without modification of the exponent.

Integral numbers are normally represented with the exponent $+24$, whereby the rightmost digit of the number falls into the last place of the numerical part of a register.

No built-in operation is needed to extract the integral part of a number (53 is the integral part of 53.67), as this may be done by adding to the number a zero with the exponent $+24$ (an "integral zero"); for in an addition the number having the smaller exponent is shifted to the right until both exponents are equal to $+24$, and a number with the exponent 24 is an integral number.

Sequencing and Coding.—Instructions for the machine are written in the form: n A op. signs B C D, where A and B are the addresses of the two numbers that are combined by the operation "op," which may be T (transfer), A (addition), M (multiplication), or E (special operations on one number only). The "signs" symbol indicates which one of the four possible combinations of signs should be attached to the numbers A and B. The different types of transfers are also distinguished by means of the "signs" symbol, whereas the different E-operations are distinguished by means of the B-address. The letter C is the address where the result should be sent, while n is the number, or index, of this particular instruction and D is the number of the next instruction.

Instructions of this type are executed automatically by means of the control system, which has three parts: the central control unit (built into the control table), the "order chain," and the five "order panels." The order

chain contains 840 relays (later it will contain 1200) connected in such a way that one and only one relay can be operated at a time. In order to start the machine on a problem, one of these relays is operated from the control table, and the machine then proceeds to operate automatically. The central control unit now supplies voltages on five lines which pass through contacts on the operated relay of the order chain to plug holes on four of the order panels. On the order panels plugged connections are made so that the voltages reach their destinations. Three of them, coming from the A-, B-, and C-panels, operate relays in the proper registers to connect these registers to the respective busses. The two remaining voltages from the operations panel give the sign-combination and initiate the operation. When the arithmetic unit gives a back-signal to the central control unit indicating that the operation is finished, the five voltages are removed, the relay in the order chain is released, and the next relay is operated. Then the whole procedure is repeated automatically.

Normally the central control unit steps the order chain from relay n to relay $n + 1$. It is possible, however, to break this sequence by means of plugged connections on the sequence panel. This is called a jump in the program. Jumps can be made from any even instruction to any odd instruction. With this restriction only, the whole of the 840 available instructions may be divided into an arbitrary number of subsequences of arbitrary length. These may constitute one or several independent computing programs. Conditional jumps are obtained by means of the selectors which will be discussed below.

The even-odd rule makes it sometimes necessary to insert meaningless instructions in the program. For instance, at the end of a subsequence that would otherwise contain an odd number of instructions, a special phony instruction is available to permit the jump.

No instructions are given to the machine from tapes or similar devices; all programs are physically realized by the plugged connections. For every instruction, normally one such connection must be made on each panel. The principle of the arrangement is similar to the subsequence mechanisms used with Mark I at Harvard and to the corresponding equipment in the BTL computer, Model VI.

Flexibility in the coding is obtained by the use of "selectors" or relay pyramid circuits. There are four 64-selectors (pyramids with 64 exits) and 125 two-way selectors. By letting the path of the corresponding plugged connection go through such a pyramid, any part of an instruction may be subject to a choice of up to 64 different possibilities. The choice is then dependent on some control number previously sent from the arithmetic circuits to the controlling relays of the pyramid. This technique greatly reduces the number of instructions needed in a program. For instance, the multiplication of two square matrices of unspecified order n (where $n < 50$) may be programmed with only 18 instructions.

Other Equipment.—Input and output devices make use of standard teletype equipment. Five tape readers, five tape punches, and one page printer are available. This equipment may also be used as external storage, although with limited flexibility, as no provisions have been made for "hunting" on the tapes. Numbers may be read or punched in binary or decimal notation and printed in octal or decimal notation. Printing in octal

form is used for checking, especially for checking of the setting of the constant registers. Conversion from binary to decimal notation, or inversely, is done by the computer itself and is programmed by ordinary means.

The operation of the machine is supervised from the control table. For checking purposes the order chain may be stepped manually, one instruction at a time, as slowly as desired. Indicator lamps then show at every instant the instruction just carried out, the addresses and operation involved, and the numbers which at that moment occur on the number transfer busses. It is also possible to step the machine manually through arbitrary instructions, not set up on the panels.

No circuits for automatic checking have been built into the machine, but alarms occur for a number of fundamental failures, such as a number exceeding the range of the machine, a dangerous drop in supply voltage, a blown fuse, and, of course, the failure of a coded check.

The machine contains in all some 5000 relays of standard telephone type. The relays are mounted in boxes which can easily be replaced by duplicate units in the case of a breakdown.

A general view of the BARK is shown in the frontispiece. In front is seen the control table and the input and output equipment. At the right and in the first row are the order panels. In succeeding rows are shown the order chain, arithmetic circuits, relay registers, and constant registers. The three empty relay racks provide space for future additions to the machine.

A block diagram of the BARK is shown in Figure 1. Thin vertical lines represent the paths of the signals that initiate operations and effect the connection of the registers to the busses. RA, for example, indicates the path of a signal coming from the A-panel, which connects one of the 50 relay registers to the A-bus.

Operation Times.—The times for elementary operations are:

Transfer	100 milliseconds
Addition	150 milliseconds
Multiplication	250 milliseconds
Printing of one digit	160 milliseconds

The efficiency under realistic conditions may probably be better judged by the following short data from some of the computations which were done during the testing period.

1. Tabulation of four 7th-degree polynomials in two variables (origin: atomic physics). Some 500 values were computed; the machine time was three hours.

2. Tabulation of the specific volume v of water-vapor as a function of the pressure p and temperature $T = 100t$ according to the formula:

$$v = RTp^{-1} - At^{-2.82} - p^2(Bt^{-14} - Ct^{-31.6})$$

R, A, B and C are constants. Some 9000 values were computed: the machine time was 70 hours.

3. Tabulation of irregular solutions of the equation

$$y'' + \left(1 - \frac{2a}{x}\right)y = 0$$

for different values of the parameter a, and $0.05 \leq x \leq 1$ (origin: atomic physics). The equation was solved with step-wise integration, using TAYLOR's series up to and including terms of 7th order, and the result was accurate within one or two units in the 6th decimal place for most values of a. The functions y and y' were computed for about 3000 points. The machine time was 42 hours. The table will be published by C-E. FRÖBERG in *Arkiv för Fysik*.

4. Solution of symmetrical systems of linear equations with the GAUSS' elimination method (origin: surveying). Matrices of orders $n = 8, 14, 20$, and 28 were treated. The machine time for $n = 28$ was 4.8 hours.

5. Inversion of symmetrical and unsymmetrical matrices of orders $n = 8$ and 20 with JORDAN's method (origin: surveying). The machine time for $n = 20$ was 7.5 hours.

Conclusion.—It was found that the coding on BARK is on the whole straightforward and easy. Flow-diagrams, of the type described in the reports on the computing machine under development at the Institute for Advanced Study, Princeton, N. J., are excellently suited for the planning of programs. The plugging of the order panels is time-consuming (the approximate speed being 50 instructions an hour) but may on the other hand be done while the machine is working on some other problem. The greatest advantage of the sequencing system is its flexibility—at any point in a computation the machine may be stopped and the program modified, e.g., by the insertion of a new instruction or subsequence or by skipping another.

The cost of the machine, including planning, designing, construction, and experimental work, does not exceed 100,000 dollars. The main bulk of the design work was done by HARRY FREESE and GÖSTA NEOVIUS. The machine was built by the Swedish Telegraph Administration, which also supplied most of the parts. Under the direction of Dr. Palm, the following persons participated in the general planning, design, and experimental work: C-E. FRÖBERG, O. KARLQVIST, G. KJELLBERG, B. LIND, A. LINDBERGER, P. PETERSSON, and M. WALLMARK.

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DISCUSSIONS

Notes on Numerical Analysis—3
Solution of Differential Equations by Recurrence Relations

1. Introduction.—J. TODD[1] has recently drawn attention to the use of recurrence relations for the numerical solution of differential equations. The characteristic feature of such processes is that successive values of the required solution are computed from earlier values by a recurrence relation involving no estimation. In his note Todd discussed the building-up errors that occur with some of these methods. Though the particular example of catastrophic building-up error given by him is in no way a general criticism of recurrence methods (since the formula in question would be unlikely to be used in actual computation), it is nevertheless true that the problem of building-up error is a serious one with these, as with all methods of solution.

This problem will be dealt with in a later note: the object of the present note is to present some observations on techniques which have arisen in the course of applications of recurrence methods to a variety of equations.

The notes below all concern the application of the "difference-correction" methods described by L. Fox & E. T. Goodwin.[2] These methods have been found to be efficient ones to employ when applicable, from the point of view both of the amount of labor involved and of the smallness of the associated building-up error. For convenience only second-order equations are treated but similar considerations hold for equations of other orders.

2. The η-process.—Consider the solution of the equation

$$(1) \qquad y'' + f(x)y = 0,$$

for a chosen interval of integration h. For convenience we take as the initial conditions,

$$(2) \qquad y(x_0) = a, \qquad y(x_0 + h) = b,$$

reserving the more usual case until section **4**. Method VII of Fox & Goodwin is based on the recurrence relation

$$(3) \qquad (1 + \phi_1)y_1 = (2 - 10\phi_0)y_0 - (1 + \phi_{-1})y_{-1} + \Delta y_0,$$

where $\phi(x) = \frac{1}{12}h^2 f(x)$, Δy is given by

$$(4) \qquad \Delta y = \left(-\frac{1}{240}\delta^6 + \frac{13}{15120}\delta^8 - \frac{17}{100800}\delta^{10} + \frac{1}{29700}\delta^{12} - \cdots \right) y,$$

and the subscripts -1, 0, 1 applied to y and ϕ are taken to represent any three successive points at the interval h.

This recurrence relation is solved by an iterative process. A first approximation $y^{(1)}$ is obtained by neglecting the difference correction. The latter is then estimated from the differences of $y^{(1)}$ and used in (3) to obtain a second approximation $y^{(2)}$. This process is continued until no further changes occur.

A variation of this technique is the calculation of successive corrections rather than successive approximations, and it results in an appreciable saving of labor when desk calculating machines are being employed and many figures retained.

The second approximation $y^{(2)}$ is written in the form $y^{(2)} = y^{(1)} + \eta$, where η is the first correction and satisfies the recurrence relation

$$(5) \qquad (1 + \phi_1)\eta_1 = (2 - 10\phi_0)\eta_0 - (1 + \phi_{-1})\eta_{-1} + \Delta y_0^{(1)},$$

and the initial conditions $\eta(x_0) = \eta(x_0 + h) = 0$. The η may be calculated from these relations, and, since it will contain many fewer figures than $y^{(2)}$, its computation is correspondingly more rapid. This process can now be repeated to produce a second correction $\eta^{(2)}$ which will contain even fewer figures than η, and so on.

An apparent drawback of this procedure is that the probable building-up error is increased since y is now obtained as a sum of the first approximation $y^{(1)}$ and successive corrections η, each of which will contain its own rounding errors. However these errors are at most additive, and, even if several successive corrections are obtained, the resulting accumulation of rounding-off error will be more than compensated by the retention of one extra guarding

figure. In the more usual case, when only the first correction is significant, even this safeguard will usually be unnecessary.

This "η-process" is of general application to the solution of linear differential equations by difference-correction methods, and in the case of simultaneous linear equations, simultaneous corrections can be obtained in a similar way.

3. Non-linear Equations.—Though the η-process is useful when employed in this way it is of much greater value in the solution of non-linear differential equations. Consider the differential equation

$$(6) \qquad\qquad y'' + f(x, y) = 0.$$

This equation can be solved very readily by Method VI of Fox & Goodwin's paper, which leads to the recurrence relation

$$(7) \qquad\qquad y_1 = 2y_0 - 12\phi(x_0, y_0) - y_{-1} + \Delta y_0,$$

where $\phi(x, y) = \frac{1}{12}h^2 f(x, y)$ and Δy is given by

$$(8) \qquad\qquad \Delta y = \left(\frac{1}{12} \delta^4 - \frac{1}{90} \delta^6 + \cdots \right) y.$$

Method VII is much more powerful, however, in the sense that it involves a very much smaller difference correction. The recurrence relation is

$$(9) \quad y_1 + \phi(x_1, y_1) = 2y_0 - 10\phi(x_0, y_0) - y_{-1} - \phi(x_{-1}, y_{-1}) + \Delta y_0,$$

where Δy is given by (4).

A direct application of equation (9) involves the solution at each step of a non-linear equation for y_1, usually best performed by a method of successive approximation such as Newton's rule, and this rather awkward process has to be repeated for each approximation. By employing the η-process, however, it is usually possible to determine the correction η to an approximate solution $y^{(1)}$ from a *linear* recurrence relation as follows.

The first approximate solution $y^{(1)}$ is obtained by using (9) replacing Δy_0 by zero. Writing

$$(10) \qquad K_1 = 2y_0^{(1)} - 10\phi(x_0, y_0^{(1)}) - y_{-1}^{(1)} - \phi(x_{-1}, y_{-1}^{(1)}),$$

the equation to be solved for $y_1^{(1)}$ at each step is

$$(11) \qquad\qquad y_1^{(1)} + \phi(x_1, y_1^{(1)}) = K_1.$$

If $a^{(1)}$, $\phi(x_1, a^{(1)})$ are taken as approximations to $y_1^{(1)}$, $\phi(x_1, y_1^{(1)})$ respectively, then the next approximations are

$$(12) \qquad\qquad a^{(1)} + \delta a, \quad \phi(x_1, a^{(1)}) + \delta a \phi_y'(x_1, a^{(1)}),$$

where

$$(13) \qquad \delta a = [K_1 - a^{(1)} - \phi(x_1, a^{(1)})]/[1 + \phi_y'(x_1, a^{(1)})].$$

If $a^{(1)}$ is correct to k figures the new approximations (12) will generally be correct to $2k$ figures. A good first approximation $a^{(1)}$ can be extrapolated from the differences of $y^{(1)}$, so that in practice only one application of (13) is necessary.

To obtain the second approximate solution $y^{(2)}$, write $y^{(2)} = y^{(1)} + \eta$ as before. Then η satisfies the recurrence relation

$$(14) \quad [1 + \phi_y{}'(x_1, y_1{}^{(1)})]\eta_1 = [2 - 10\phi_y{}'(x_0, y_0{}^{(1)})]\eta_0$$
$$- [1 + \phi_y{}'(x_{-1}, y_{-1}^{(1)})]\eta_{-1} + P + \Delta y_0{}^{(1)},$$

where P comprises terms involving second and higher powers of η. The quantity $\phi_y{}'(x_1, y^{(1)})$ will already have been tabulated to a sufficient accuracy during the calculation of $y^{(1)}$. Thus, if P is neglected, η can be rapidly computed from a linear recurrence relation. The value of P can subsequently be estimated, and, if necessary, its effect, and also that of $\Delta\eta$, can be allowed for by a further correction $\eta^{(2)}$, though in all the examples on which we have employed this method P and $\Delta\eta$ have both turned out to be negligible. When subsequent reference is made to (14), it will be assumed that P is negligible.

4. Initial Conditions Involving the Derivative.—In the above discussion it has been supposed that two consecutive initial values of the required solution have been available. Frequently, however, the initial conditions may involve the derivative, taking the form

$$(15) \qquad y(x_0) = a, \qquad hy'(x_0) = c.$$

For a linear differential equation this case usually presents little difficulty since $y(x_0 + h)$ can be obtained from the Taylor series at x_0, the successive derivatives being obtained by repeated differentiations of the equation. With a non-linear equation, however, this process may be a tedious one, due to the difficulty of obtaining the higher derivatives. Though it is always possible to use a very small interval it is generally preferable to use an extension of the "η-process" by means of which most of the higher derivatives can be avoided entirely without reduction of the interval.

Suppose for example it is desired to carry out the integration to ten decimals in y and that throughout the range of integration it is known that $|\phi_{yy}''(x, y)| < 0.1$. In these circumstances the Taylor series is used to determine $y(x_0 + h)$ accurately to *five* decimals only, and, if the value so obtained is denoted by β, then starting with the initial values

$$y^{(1)}(x_0) = a, \qquad y^{(1)}(x_0 + h) = \beta,$$

a first approximate solution $y^{(1)}$ is obtained to ten decimals from the recurrence relation (9), replacing Δy_0 by zero. The solution $y^{(1)}$ is extended for two or three backward steps of the argument from x_0 and the value of $h(dy^{(1)}/dx)$ at $x = x_0$ is determined by central numerical differentiation. Clearly the required solution of the differential equation will be $y^{(1)} + \eta$ where η satisfies (14) and has the initial values

$$(16) \qquad \eta(x_0) = 0, \qquad h\eta'(x_0) = c - h(dy^{(1)}/dx)_{x=x_0} = d.$$

Thus the original problem of starting the solution of the equation for y with the conditions (15) is now replaced by an exactly similar problem for η with the conditions (16). The advantage of transforming the problem into this form lies of course in the fact that the recurrence relation satisfied by η is a linear one.

The actual starting of the η-integrations can be carried out as follows. Let $\eta^{(1)}$ be any particular solution of (14) such that $\eta^{(1)}(x_0) = 0$ and let η^* be any solution of

$$(17) \quad [1 + \phi_y{}'(x_1, y_1{}^{(1)})]\eta_1 = [2 - 10\phi_y{}'(x_0, y_0{}^{(1)})]\eta_0$$
$$- [1 + \phi_y{}'(x_{-1}, y_{-1}^{(1)})]\eta_{-1},$$

such that $\eta^*(x_0) = 0$, $\eta^*(x_0 + h) \neq 0$. Then all the solutions of (14) which vanish at $x = x_0$ can be written in the form $\eta = \eta^{(1)} + A\eta^*$, where A is an arbitrary constant. The solution satisfying (16) has A given by $A = (d - d_1)/d^*$, where $d_1 = h(d\eta^{(1)}/dx)_{x=x_0}$, $d^* = h(d\eta^*/dx)_{x=x_0}$, and can be determined by numerical differentiation. Thus the initial values of the desired η can be obtained by constructing numerically two solutions $\eta^{(1)}$, η^* of (14) and (17) respectively in the neighbourhood of $x = x_0$ and forming their appropriate linear combination. For convenience $\eta^{(1)}$ is chosen to be as near the true η as possible, for example the value of $\eta^{(1)}(x_0 + h)$ could be taken as d.

5. Examples.—Non-linear differential equations of the type (6) that have recently been solved at the Mathematics Division by application of difference-correction methods have been the differential equation for the modulus of the Hankel function $H_n{}^{(1)}(x)$ and Emden's equation. The former of these is required incidentally in the computation of the early zeros of the Bessel functions $J_n(x)$, $Y_n(x)$; its application in this connection is described fully elsewhere.[3] The actual equation which is solved numerically is

$$(18) \qquad \frac{d^2u}{dx^2} = \frac{\pi^2}{u^3} - \frac{x^2 - n^2 + \frac{1}{4}}{x^2}\, u,$$

the desired analytical solution being

$$u = 2^{-\frac{1}{2}}\pi x^{\frac{1}{2}}[J_n{}^2(x) + Y_n{}^2(x)]^{\frac{1}{2}}.$$

Integrations of (18) were carried out to eleven decimals in u over the range $n \leqslant x \leqslant n + 5\pi$, the interval in x being $\frac{1}{4}$ or $\frac{1}{2}$. One run with the recurrence formula (9) with Δy_0 replaced by zero, followed by a single application of the "η-process," produced the required solution u correct to eleven decimals. Initial values $u(n)$, $u'(n)$ were obtained from asymptotic expansions and the integrations were in effect started by the device described in the previous section. An analysis of the recurrence relations indicated the building-up error in u to be of an oscillatory nature and of magnitude not exceeding about three or four units in the eleventh decimal. This was verified in one or two instances by repeating the solution retaining a different number of decimals.

Emden's equation can be written in the form

$$\frac{d^2z}{dx^2} + x\left(\frac{z}{x}\right)^n = 0,$$

and solutions of this for $n = 1\frac{1}{4}(\frac{1}{2})4\frac{3}{4}$ with the initial conditions $z(0) = 0$, $z'(0) = 1$, have been prepared for the Royal Society Tables Committee over the ranges $0 \leqslant x \leqslant x_0$ where x_0 is the first zero of z. The number of steps

involved increases with n and varied from about 30 to 150. Ten decimals were retained in z for the lower values of n and eleven for the higher values. The building-up error here was more severe than that associated with the equation (18), but even so, at least eight decimal accuracy could always be guaranteed in z. Again one run of (9) taking the difference correction as zero, followed by a single application of the "η-process," was adequate to produce the solution z to the requisite accuracy.

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[1] J. TODD, "Solution of differential equations by recurrence relations," *MTAC*, v. 4, p. 39–44.

[2] L. FOX & E. T. GOODWIN, "Some new methods for the numerical integration of ordinary differential equations," Cambridge Phil. Soc., *Proc.*, v. 45, 1949, p. 373–388.

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This is a brief note on the development at the Bell Telephone Laboratories of a method for endowing high-speed computers with a self-correcting faculty.

2. ANON., "Electronic computers," I. R. E., *Proc.*, v. 38, Apr. 1950, p. 373–375.

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3. ANON., "New memory tube," *Electronics*, v. 23, May 1950, p. 130.

A new electrostatic storage tube developed at Massachusetts Institute of Technology was announced at the IRE convention in New York last March.

It is a beam-deflection tube which stores binary information at two stable potentials, 100 volts apart. A 100-volt electron flood replaces leakage and maintains the stored information indefinitely. A single 2,000-volt electron beam writes or reads one of 400 binary digits on a four-inch target. The potential boundary is kept stable on the storage surface by a mosaic of conducting beryllium squares. The access time is 25 μ sec. At the present time tubes are in pilot production for use in a digital computer. It is hoped that future developments will decrease access time to 6–12 μ sec. and increase storage capacity to 1,024 binary digits.

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NBSMDL

4. ANON., *Swedish Automatic Relay Computer*, July 20, 1950, 4 pages, mimeographed, Office of Naval Research, London, Technical Report ONRL-67-50.

The report presents a brief description of the recently completed Swedish relay machine, Binär Automatisk Relä-Kalkylator or BARK [*MTAC*, v. 4, p. 53, 118, v. 5, p. 29–34].

5. ANON., NBS, *Technical News Bulletin*, v. 34, Sept. 1950, p. 121–129.

Included in this issue is a description of the National Bureau of Standards Eastern Automatic Computer (SEAC) including sections on the solution of the skew-ray problem (SEAC's first application in the physical sciences), on the solution of a heat-flow problem, and on the NBS computer program.

6. M. L. BYKHOVSKIĬ, "Osnovy electronykh matematicheskikh mashin discretnovo scheta" (Principles of electronic mathematical digital computing machines), *Uspekhi Matematicheskikh Nauk*, v. 4, 1949, p. 69–124.

Although this article gives a full account of several machines already constructed or in the process of construction—in the United States and England, no mention is made of these facts, nor is any machine alluded to by name. The article is replete with diagrams, photographs, and charts taken from publications in this country and in England, but no mention is made of their sources. The ENIAC and SSEC designs are treated in great detail, and much space is given to a description of various memory devices, including the Selectron and the Williams memory tube. The only Russian contribution that the reviewer could find was a reference to G. B. VOĬTILLA's textbook entitled, *A General Course in Radiotechnology*, Moscow, 1948.

IDA RHODES

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7. R. W. HAMMING, "Error detecting and error correcting codes," *The Bell System Technical Journal*, v. 29, 1950, p. 147–160.

This paper is divided into two main parts. The first part explains principles for designing error detecting and correcting codes for binary equipment, with emphasis on (a) single error correcting codes and (b) single error correcting and double error detecting codes.

The use of such codes may be illustrated by the single error correcting code. In this kind of code we assume the code symbols to be n binary digits in length, m digits of which are associated with the information while $k = n - m$ digits are used for detection and correction of a single error. Having received a code symbol, we derive from it a k-position "checking number" (to be distinguished from the k error detecting and correcting positions in the code symbol as transmitted) which will be 0 if the number received is correct in all n positions. If the received number is incorrect in a single digit position, the checking number indicates the position. The author also derives criteria for the "redundancy" $R = n/m$ to be a minimum.

The second part of this paper discusses the general theory of error detecting and correcting codes in terms of a geometric model. If we assume a code requiring n binary digits, the model consists in setting up a corre-

spondence between the code symbols and the corresponding vertices of a unit n-dimensional cube. The code points form in general a proper subset of the set of all vertices of the cube. "Distance" between two points in this space of 2^n points is defined as the least number of edges which must be traversed in going from one point to the other. This distance function satisfies the conditions for a metric. Criteria are developed for single error detection, single error correction, single error correction plus double error detection, etc., in terms of minimum "distance" between code points. The previously derived conditions for minimum redundancy are again derived by use of the geometric model.

<div align="right">Joseph H. Levin</div>

NBSCL

8. James H. Knapton & Louis D. Stevens, "Gate-type shifting register," *Electronics*, v. 22, Dec. 1949, p. 186–192.

This shifting register is most notable for its economy of components. Each stage contains only one double triode, eleven resistors, five capacitors, and two germanium diodes connected to form an Eccles-Jordan type flipflop and two simple gate circuits. Shift pulses are applied simultaneously to every grid of every stage, but each is gated by the potential of the corresponding plate of the preceding stage. Thus the necessary memory for the information in transit resides in the plate capacitances, because to gate the shift pulse for the next stage a plate must maintain its former potential throughout the duration of an effective flipping pulse on the grids. The gate circuits are amplitude sensitive in the sense that a shift pulse that is too large can override gating by the plate potential. This register has shifted at 600 kc. and is said certainly to shift reliably up to 250 kc. While shifting registers which are both faster and which deliver more useful output current per stage have been built, the economy of this circuit may, for suitable applications, offset these as well as the disadvantages of amplitude sensitive gating.

<div align="right">R. D. Elbourn</div>

Electronic Computers Section
NBS

9. Moore School of Electrical Engineering, *A Functional Description of the EDVAC*. 2 v., Philadelphia, 1949, University of Pennsylvania, Mimeographed.

This publication is a two-volume report including 20 pages of preface and a table of contents, 212 pages of text, 73 pages of appendices, and 47 drawings. A list of the authors is included on page II of the preface.

The text is divided into nine chapters. These are: (1) Introduction, (2) Dispatcher, (3) The EDVAC Control, (4) Computer, (5) Memory, (6) Reader-Recorder, (7) Timer, (8) Power Supply, and (9) Switchgear.

There are five appendices, which are: (1) Physical Description, (2) List of Remote Connections, (3) Definitions and Abbreviations, (4) General Principles of Crystal-Diode Gating Circuits, and (5) EDVAC Drawings.

The purpose of this report can best be stated by quoting three sentences from page III of the preface. "It is believed that personnel assigned to the maintenance of the EDVAC will find this logical or functional description

of much greater value in their work than a circuit analysis. It is hoped that this report will offer more than an aid to maintenance. It contains a description of the pulse and logical techniques used in the EDVAC and thus will prove of interest to all those in the digital computing and allied fields."

As far as content is concerned, Chapter 1 contains a short description of the various units comprising the EDVAC, as well as a summary of the codes used and the speeds at which various functions are performed. Chapter 2 discusses the circuits used to interpret the coding and to supply operating pulses to the computer, as well as the halt circuitry, the extract circuitry, and the memory systems necessary for the dispatcher. Chapter 3 covers the buttons, lights, and switches by which the operator controls the EDVAC. This chapter also explains both the circuits controlled by the buttons and switches and those controlling the lights. Chapter 4 describes the computing unit, the circuits used in the basic arithmetic operations, the "carry" and "borrow" circuits, and the computer check circuits. Chapter 5 discusses the memory tanks and the circuits used in reading numbers into and out of the memory. Chapter 6 covers the reader-recorder equipment (not completed at the time of publication), the circuits to be used in reading from the magnetic tapes to the EDVAC, and the circuits reading information from the EDVAC to the magnetic tapes. Chapter 7 describes the timer and the circuits used to synchronize the operations of the various units of the EDVAC. Chapter 8 describes the power supply and the voltage regulating circuits. Chapter 9 discusses the switches which control the application of power to the EDVAC and the fuse and thermocouple safety systems.

Appendix 1 describes the physical size and layout of the EDVAC, gives some statistics on the number of tubes, crystals, and other basic components used, and lists the lettering system used to identify any particular pin on any plug of any chassis. Appendix 2 lists all the remote connections—pulses used on any drawing which do not originate on that drawing and the drawings on which they originate. Appendix 3 lists the abbreviations used and defines many of the electronic terms used in the report. Appendix 4 discusses in some detail the theory of crystal gating, particularly for those gates used in the EDVAC. Appendix 5 lists the drawings included in the report and explains the system of numbering drawings.

The report is completely built around the 47 logical drawings included at the end of the text. It should be emphasized that these are not circuit drawings with all the details of tubes and resistors and condensers necessary to construct the machine, but rather logical drawings in terms of "and" circuits, "on" circuits, and "inhibitors" which show how the machine makes its necessary decisions. It is impossible to read intelligently any of the chapters of the main report, except Chapter 1, without constant reference to these drawings. However, by carefully following text and drawings simultaneously, the logic of the circuits is completely explained and not too difficult to follow.

The text itself was written by several authors, each writing one chapter. It suffers in some respects from lack of proper editorial supervision. The early chapters are written using a completely logical notation which ignores all specific circuit elements. The last sentence of Chapter 6 reads, "PAcc F4C4 that energizes Ff F4C3 controlling /WM/ output only searches for a pulse in PP32 by requiring coincidence between /ZC/ and a command

pulse at time 32." The following sentence, taken from page 8–4, is typical of the later chapters: "In the 6J6 plate circuit a resistor network provides a d.c. stepdown to vary the bias of a type 6AC7 pentode d.c. amplifier." There may be a good reason for this shift to specific detail, but it is not apparent. This change was quite confusing, particularly as the diagrams accompanying these sections were detailed circuit diagrams rather than logical diagrams. Also, many of the early chapters were far too long for the amount of explanation contained therein.

This report undoubtedly fulfills its first purpose. The machine is completely described in a manner well suited for maintenance work. It falls short on its other objectives. As far as pulse techniques and logical techniques go, there is little of pulse techniques and a not-too-adequate summary of the logical techniques used in the EDVAC. It will be of interest primarily to persons working in the field of machine design and construction and of little interest to persons using machines to solve problems.

EVERETT C. YOWELL

NBSINA

10. GEORGE W. PATTERSON, *Bibliography of Unclassified Moore School Reports on Electronic Digital Computers*, Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, 1950, 3 p.

11. OFFICE OF NAVAL RESEARCH, *Digital Computer Newsletter*, v. 2, no. 3, August 1950, 3 p.

The present status of the following digital computer projects is treated briefly in this number.

1. The Aberdeen Proving Ground Computers
2. The Institute for Advanced Study Computer
3. National Bureau of Standards Eastern Automatic Computer (SEAC)
4. National Bureau of Standards Western Automatic Computer (SWAC)
5. Project Whirlwind
6. MADDIDA
7. Raytheon Computers
8. The EDSAC, Cambridge University, England

12. AN WANG & WAY DONG WOO, "Static magnetic storage and delay line," *Jn. Appl. Phys.*, v. 21, 1950, p. 49–54, figs.

Several years ago HOWARD AIKEN, Director of the Computation Laboratory at Harvard University, proposed a memory device which does not require a continual supply of power to maintain storage. It is a magnetic core that may be in either of two states of residual induction according to the direction in which it was last saturated. The state of the core may be sensed by pulsing it strongly. If the residual induction was already in the direction of the pulse, the induction will change very little; but, if the residual induction was in the opposite direction, the pulse will reverse the induction, and this large change can induce a pulse in another winding. With a suitable coupling circuit using one or two resistors or selenium rectifiers, the state of one core can be transferred to another by the sensing pulse which thus

becomes a shifting pulse. In this manner magnetic flipflops and shifting registers (delay lines) can be built. Work on these devices under contract W19-122-AC-24 with the U. S. Air Force has been reported regularly in the quarterly progress reports of the Computation Laboratory and is well summarized in this paper.

The speed of reversing the induction in a core is limited by eddy currents; hence the time for reversing varies directly with the lamination thickness and inversely with the impressed voltage. For 0.001 inch thick laminations of 50% nickel-iron alloy and a reasonable impressed voltage the reversing time is 10 microseconds; therefore, the shifting frequency is limited to 30 or 50 kc.

The recently announced commercial availability of magnetic strip 0.00016 inch thick (see *Iron Age*, Aug. 10, 1950, p. 90) may permit some increase over the speed reported in this paper. The factor of six in thinness might be expected to produce an increase in speed by the same factor; however, before this factor is achieved, leakage inductance and stray capacitance will become so significant as to require a more careful analysis of the device's operation.

R. D. ELBOURN

Electronic Computers Section
NBS

13. M. V. WILKES & W. RENWICK, "The EDSAC—an Electronic calculating machine," *Jn. Scientific Instruments and of Physics in Industry*, v. 26, 1949, p. 385–391.

NEWS

Association for Computing Machinery.—The fall meeting of the Association was held on Sept. 7 through 9 in Washington, D. C. In addition to the meetings, there was a demonstration of the National Bureau of Standards Eastern Automatic Computer (SEAC) at the National Bureau of Standards Electronics Laboratory.

The program for the meeting was as follows:

September 7, Evening Session	J. H. CURTISS, NBS, *Chairman*
"The impact of high-speed computing on atomic research"	R. D. HUNTOON, NBS
September 8, Morning Session	R. F. CLIPPINGER, BRL, *Chairman*
"The federal computing machine program"	MINA REES, Office of Naval Research
"High-speed computation in programming and planning"	J. VON NEUMANN, Institute for Advanced Study
"The effect of high-speed computing on mathematical research"	D. H. LEHMER, University of California, Berkeley
Afternoon Session (A)	M. V. HANSEN, Bureau of the Census, *Chairman*
"Remote control demonstration of the SEAC"	R. J. SLUTZ, NBS
"Operational experience on the EDSAC"	M. V. WILKES, University of Cambridge
"A photographic high-speed printer (300–3000 characters per second)"	H. L. DANIELS, Engineering Research Associates, Inc.
"Provision for expansion of the SEAC"	A. L. LEINER, NBS

Panel discussion on the potentialities and the need for electronified filing and records systems. Participants:

R. R. Shaw, Department of Agriculture
M. E. McGeoghegan, Department of Treasury
J. Rabinow, NBS
D. Savage, Remington Rand, Inc.
I. Travis, Burroughs Adding Machine Co.
H. L. Daniels, Engineering Research Associates, Inc.

Afternoon Session (B)	C. V. L. Smith, Office of Naval Research, *Chairman*
"Number-theoretical problems on the SEAC"	J. C. P. Miller, NBS
"On the numerical solution of one-dimensional aerophysical problems involving shocks"	R. J. Seeger & H. Polachek, U. S. Naval Ordnance Laboratory
"Numerical methods in the theory of linear partial differential equations of elliptic type"	S. Bergman & M. M. Schiffer, Harvard University
"Some recent experiments with the Monte Carlo method"	J. Todd, NBS
"Application of the SEAC to linear programming"	G. B. Dantzig, Office of the Air Comptroller, USAF
September 9, Morning Session	E. W. Cannon, NBS, *Chairman*
"Operational experience on the EDSAC (Part II)"	M. V. Wilkes, University of Cambridge, England
"Applications of high-speed computing in aeronautical research"	H. L. Dryden, National Advisory Committee for Aeronautics
"The role of a central computing laboratory"	J. H. Curtiss, NBS
Afternoon Session	E. D. Schell, Office of the Air Comptroller, USAF, *Chairman*
"Integrating systems of ordinary differential equations"	L. H. Thomas, IBM
"Additive constants in machine programs"	M. H. A. Newman, University of Manchester, England
"On the non-iterative numerical solution of boundary value problems"	M. A. Hyman, U. S. Naval Ordnance Laboratory
"Some thermodynamic tables obtained on punched-card machines"	J. Belzer, The Ohio State University
"The determination of a potential using the Fairchild Linear Equation Solver"	C. L. Perry, Oak Ridge National Laboratory

Institute for Applied Mathematics of the Swiss Federal Institute of Technology.—In July 1950 a sequence controlled computer was installed at the Institute located in Zurich. The computer, which is similar to the Bell Computer Model 5, was constructed by Konrad Zuse with the collaboration of the Institute. (See *MTAC*, v. 2, p. 355–359 for an earlier description of the Zuse computer.)

This relay computer uses 2200 telephone relays and 20 stepswitches and contains a new type of mechanical storage element developed by Zuse. At present the machine has a storage capacity of 64 numbers with an access time of .5 sec. It is hoped that the capacity will eventually be increased to 1024 numbers.

It is a binary computer with a floating binary point and with the binary exponent ranging in value from $+63$ to -64. Binary to decimal conversion is fully automatic. The machine has the special faculty of handling values such as 0, ∞, and $\frac{0}{0}$ by the storage and arithmetical unit to prevent machine stoppage due to an overflow.

The computer is essentially a one-bus machine, each order containing an operation or an operand. Input is accomplished by a ten-place keyboard or by punched tape; output is typewritten or punched on tape which can be refed to the tape reading unit thus providing an external storage.

The following orders are performed on the machine: add, subtract, multiply, divide, square root, form absolute value, conditional and unconditional call, conditional and unconditional stop, and conditional skip. (The skip order causes all the following orders up to a starting order to be disregarded and hence permits several subsequences to be punched on one loop of tape.) The total times for addition and subtraction, multiplication, and division and square rooting are approximately .1 sec., 2.5 sec., and 6 sec., respectively. To skip an order requires .2 sec.

A problem preparation unit similar to the coding machine for Mark III has been used in preparing the sequence tape. Unlike the coding machine, the keyboard for this unit can be used to operate the computer manually. The coded sequence is punched into movie film (each order being 8 binary digits in length). This is fed into one of the two reading stations. Provisions are now made for additional reading stations.

Institute for Numerical Analysis.—On August 17, 1950, the National Bureau of Standards Western Automatic Computer (SWAC) was formally dedicated at the Institute, University of California, Los Angeles. The machine was sponsored by the Office of Air Research of the United States Air Force for use by the Institute in long-range mathematical research as well as on present-day problems originating with the Air Force, Air Force contractors, and other governmental agencies. Two primary functions of the Institute are to carry on long-range fundamental research in various fields of mathematics related to the effective use of automatic digital computing machinery and to provide computing services to western scientific laboratories. The research program is financed principally by the Office of Naval Research while the computation unit is financed chiefly by the Office of Air Research. The completion of SWAC greatly improves the computing facilities of the Institute and increases the effectiveness of the research program. (For a description of SWAC, see *MTAC*, v. 4, p. 103–108.) Speakers at the dedication ceremonies were E. U. CONDON, NBS; Col. F. S. SEILER, OAR; L. N. RIDENOUR, Univ. of Ill.; J. H. CURTISS, NBS; and H. D. HUSKEY, INAMDL. The ceremonies were followed by a demonstration of the SWAC.

The SWAC is an extremely fast (16,000 additions of ten-digit numbers and 2,500 multiplications per second) automatically sequenced electronic digital computer. Cathode ray tubes operating on a principle discovered by F. C. Williams of Manchester University, England, are used as the storage element in the high-speed memory unit. This unit is parallel with (initially) thirty-seven binary digits per word or number. Its access time is 16 μ sec. This type of memory requires regeneration, which is accomplished during alternate eight-microsecond intervals. During the other eight-microsecond intervals, operands are transferred from the memory to the arithmetic unit, results are transferred back to the memory, and the next command is transferred to the control unit.

The arithmetic unit also operates in parallel fashion. The net addition time, about five microseconds, is determined by the time required for carry to take place in respect to all of the thirty-seven digits of the word. The computer operates in a synchronous manner, the full five microseconds being allowed for each addition whether carry takes place or not.

The arithmetic unit performs the operations of addition, subtraction, both rounded off and exact multiplication, normal and absolute comparison (which changes the course of the computation depending on the relative sizes of two numbers), and extract (which divides numbers up into parts which the computer can then handle in different ways). More elaborate operations than these are accomplished by routines of instructions stored in the memory.

The initial input-output equipment consists of electromatic typewriters and punched paper tape units. Routines for solving standard problems will be established on tape and stored in a "library."

An auxiliary memory of a magnetic drum is now being built and will be added to the computer, increasing the computer's total storage capacity to over 8000 words. A magnetic

tape input-output unit is also being added to the computer. It is to be used as a slow-speed memory and will have a capacity of about 180,000 words.

The computer and its auxiliary equipment óccupy about 50 square feet of floor space. Only standard components are used throughout the computer. All circuitry is on plug-in units, and there are spare plug-in units for about 80% of the chassis in the computer. This type of construction, together with certain borderline checking facilities, will, it is hoped, mean a small percentage of down-time for the computer.

The research computing on the machine will include such problems as matrix inversion, finding characteristic values of matrices, solution of simultaneous linear equations, finding complex roots of algebraic equations, etc. A problem in pure mathematiçs for which it is planned to use the machine is the computation of zeros of the Riemann-zeta-function. Computation of more roots would lead to further information on the distribution of primes and might provide the key steps for a proof or disproof of this famous conjecture.

The dedication ceremonies were followed on August 18th by a symposium on the applications of digital computing machinery to scientific problems. The purpose of the symposium was to interchange information on various scientific problems which are now being studied by West Coast laboratories and universities and to which high-speed automatic digital computing machinery may be applicable.

The program for the meeting was as follows:

Introductory Remarks	E. U. CONDON, Director, NBS
Morning Session	E. P. LITTLE, Office of Air Research, U.S.A.F., *Chairman*
"Initiation of an airplane turn"	ELLIS LAPIN, Douglas Aircraft
"Problems in water entry ballistics"	E. P. COOPER, U. S. Naval Ordnance Test Station, Pasadena
"Reduction of measurements in free flight testing of missiles"	ELMER GREEN, U. S. Naval Ordnance Test Station, Inyokern
"Solution of games by iterative processes"	PAUL ARMER, RAND Corporation
"Nuclear reactor physics computations"	SIDNEY H. BROWNE, North American Aviation, Inc.
"The use of iterative processes in the solution of partial differential equations"	STANLEY FRANKEL, California Institute of Technology
"A problem of the Naval Air Missile Test Center"	L. H. CHERRY, U. S. Naval Air Missile Test Center, Point Mugu
Afternoon Session	H. D. HUSKEY, NBS, *Chairman*
"Some problems in mathematical statistics"	JERZY NEYMAN, University of California, Berkeley
"An iterative construction of the optimum sequential decision procedure when the cost function is linear"	LINCOLN MOSES, Stanford University
"Problems in pure mathematics"	D. H. LEHMER, University of California, Berkeley
"On the Green's function of the clamped plate"	PAUL R. GARABEDIAN, Stanford University
"Perturbations of a satellite rocket"	SAMUEL HERRICK, University of California, Los Angeles
"Physics research problems at Stanford susceptible to automatic computation"	PAUL H. KIRKPATRICK, Stanford University
"An astronomical problem"	LELAND E. CUNNINGHAM, University of California, Berkeley
"Automatic computation in rocket engine research"	H. L. COPLEN, Aerojet Engineering Corp.

Moore School of Electrical Engineering, University of Pennsylvania.—The University is offering a graduate course for 1950–1951 in electrical engineering with emphasis on large-scale computing devices. The course of study includes the following subjects: transient circuit analysis, engineering physics, electronics, introduction in digital computing machines, engineering techniques for solving differential equations, servomechanisms and feedback control, continuous variable computers, digital computers-logic, digital computers-engineering principles, advanced topics in numerical methods for digital computers, and advanced engineering mathematics.

Swedish Board for Computing Machinery.—The Board for Computing Machinery was appointed by the Swedish Government in November 1948. At present its members are:

Rear Admiral G. Jedeur-Palmgren, Stockholm
Professor Torbern Laurent, Stockholm
Professor Edy Velander, Stockholm
Permanent Secretary Gustav Adolf Widell, Stockholm (*chairman*)
Professor Nils Zeilon, Lund.

The Board has the authority to make decisions concerning the development and acquisition of computing machinery for the Swedish State within a budgetary frame fixed by the Parliament. Its aim is to provide computational service to Swedish State agencies as well as to private institutions and enterprises.

The following persons have been appointed by the Board to act in an advisory capacity: Mr. Gunnar Berggren, Stockholm, Professor Stig Ekelöf, Gothenburg, Dr. Carl-Erik Fröberg, Lund, and Commodore Sigurd Lagerman, Stockholm.

Under the supervision of the Board, Dr. Conny Palm, Stockholm, is head of the Projects Group, within which the experimental, design, and construction work is carried out. The secretary of the Board is Mr. Gösta Malmberg, Stockholm.

The Board will issue from time to time communications in English, which will be sent to interested persons in other countries. Anyone desiring to receive these communications should write to:

Matematikmaskinnämnden
Drottninggatan 95 A
Stockholm 6.

OTHER AIDS TO COMPUTATION

Bibliography Z–XIV

14. R. Bereis, "Mechanismen zur Verwirklichung der Joukowsky-Abbildung," *Archiv für Math.*, v. 2, 1949–1950, p. 126–134.

The author considers two mechanisms which transform the $z = x + iy$ plane into itself according to the Joukowsky transformation. As an introduction, some of the well known properties of the Joukowsky transformation are summarized. By appropriate use of his mechanisms, the author shows how these transformation properties may be realized. The mechanisms discussed consist of modifications of two types of inversors. First, the author considers two Peaucellier inversors, each of which consists of a rhombus linkage. By cross-knotting these inversors, the author obtains the desired mechanism (called a "Zwillings-inversors"). The second mechanism is built up from the Hart inversor. This inversor consists of an antiparallelogram.