209.—J. V. USPENSKY, *Introduction to Mathematical Probability*, 1937.

On page 407, Table of the Probability Integral
for $\phi(z) = .499997$ *read* .500000

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UNPUBLISHED MATHEMATICAL TABLES

In this issue an Unpublished Manuscript Table is referred to in RMT **990.**

144[F].—A. GLODEN & J. BONNEAU, *Factorization of* $N^4 + 1$ *for isolated values of N between* 30000 *and* 40000. One page typewritten manuscript. Deposited in UMT FILE.

The table contains 88 factorizations, all complete. No primes are given. [For previous tables of this kind see *MTAC*, v. 2, p. 211, 252, 300; v. 3, p. 21, 118–119, 486; v. 4, p. 24; v. 5, p. 133–134.]

145[D, F].—D. H. LEHMER, *Table of Cyclotomic Cosines*. Ten manuscript pages tabulated from punched cards. On deposit in the UMT FILE. Also available on punched cards.

The table gives 20D values of

$$2 \cos 2\pi k/p \quad \text{for} \quad k = 1(1)(p - 1)/2$$

for every odd prime $p < 100$. There are 517 values in all. Thus the table gives twice the real parts of the p-th roots of unity.

146[F, L].—D. H. LEHMER, *Table of Kloosterman Sums*. Twenty manuscript pages tabulated from punched cards. On deposit in the UMT FILE. Also available on punched cards.

The table gives 19D values of

$$\text{Sp}\,(k) = \sum_{n=1}^{p-1} \exp\{2\pi i(kn + \bar{n})/p\} \quad (n\bar{n} \equiv 1 (\text{mod } p))$$

for $k = 1(1)p - 1$ and for every odd prime $p < 100$. The table was computed from UMT **145**, and contains 1034 entries. These sums appear in Fourier coefficients of many elliptic modular functions.

AUTOMATIC COMPUTING MACHINERY

Edited by the Staff of the Machine Development Laboratory of the National Bureau of Standards. Correspondence regarding the Section should be directed to Dr. E. W. CANNON, 415 South Building, National Bureau of Standards, Washington 25, D. C.

TECHNICAL DEVELOPMENTS

THE SERIAL-MEMORY DIGITAL DIFFERENTIAL ANALYZER

Introduction. In January, 1950, the first model of a digital differential analyzer became a working reality. This machine was entirely contained

in a volume of $5\frac{1}{2}$ cubic feet. The compactness, simplicity of construction, and digital accuracy of this computer by far overshadowed any differential analyzer built prior to this time.

This first machine possessed 22 integrators, each of 22 binary digit capacity.

The key to the practicality of this relatively midget computer is its serial memory which enables one network of computing circuitry, which operates on one binary digit at a time, to be shared for all computations. This computing center consists of 44 vacuum tubes and 700 diodes.

Although any type of serial memory can be used for this type of machine, the most practical memory to date is a magnetic drum because of its compactness and reliability.

It is the purpose of this paper to give a brief explanation of the logical embodiment of this type of computer and a description of some of the machines most recently designed.

General Description. The Digital Differential Analyzer can be considered in four basic sections: The control unit, the memory, the computing center, and the power supply.

The control unit provides for filling the memory with information, starting and stopping computation and for displaying memory information by means of a readout indicator. This unit also controls power. The unit can be built as a part of the computer or it can be provided as a separate unit for remote operation.

The memory is a rotating drum coated with a black magnetic oxide. With the exception of a permanently recorded clock channel, all memory channels are dynamically recorded between a read and a record head covering a sector of the drum. Appropriate amplifiers and shapers are associated with the read and record heads to develop proper signals.

Since the computer is a serial device, information, as it is read from the memory, passes through the computing center a pulse (binary digit) at a time. Here it is altered as demanded by the calculations performed and then re-recorded in the memory. The computing center is a maze of gates, inverters and flip-flops which are closely interrelated so that all computation is performed in synchronism with the memory clock.

Integrators. This computer, like all differential analyzers, is made up of fundamental integrating units, known as integrators. An individual integrator accepts two streams of digital information as a series of input pulses and releases, as an output, pulses related to the inputs by integration. Since the inputs and outputs of integrators are in the same physical form (pulses), a problem is solved by making proper electrical connections between integrators.

Consider the two registers and additive-subtractive transfer arrangement shown in figure 1. This is in essence a digital integrator in which the dy and dx of the integrator are represented by pulse rates. Likewise the output of the integrator, dz, is in the same form. If Y is added to R every time a pulse occurs on the dx line and Y is created by accumulating dy increments, this device operates such that the pulse rate out $\frac{dz}{dt} = K\left(\int \frac{dy}{dt}\,dt\right)\frac{dx}{dt} = KY\frac{dx}{dt}$ where $\frac{dy}{dt}$ is the rate of pulses accumulated

in Y and $\frac{dx}{dt}$ is the rate of Y to R addition. K is dependent on the number system used and the numerical capacity of R. [For more details see *MTAC*, v. 6, p. 41–49.]

The Memory. Recirculation or delay-type channels are used in this type of computer for the entire memory. A permanently recorded clock channel, which is closed upon itself around the drum, is used for synchronism throughout the computer and memory. (All reading and recording of memory signals and computer operations are kept in step by pulse times defined by these clock signals.)

Each incoming signal from the computer unit to the memory is first amplified and clipped in an amplifier whose plate is clamped to allow a limited swing. This insures that signals of uniform amplitude and waveform are applied to the grids of the recorder tubes. The "non-return-to-zero" method of recording is employed, whereby a record head is used to reverse a saturation pattern previously laid down by an erase head.

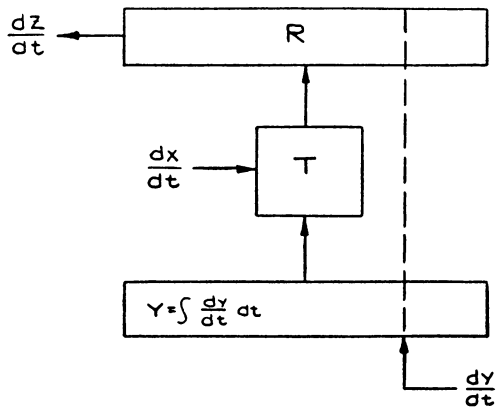

FIG. 1. Transfer device which performs digital integration.

The recorded pattern is picked up by the playback head after an appropriate delay represented by the fraction of a revolution between the record and playback heads. After detection, the signal is amplified and sent to the computer section. Here it is put into a phase inverter which gives two amplified outputs, both similar to the input signal but opposite in phase. Since the detected signal from a magnetic memory is the derivative of what was recorded, a positive pulse represents a change of 0 to 1 and a negative pulse from 1 to 0. The negative pulses from the two voltage sources of the phase inverter correspond now to these two memory changes. By passing the phase inverter signals through clippers arranged to pass only negative signals, the signals which denote changes of memory content are indicated by well-defined negative pulses. These pulses are then put unto the appropriate grids of a flip-flop (primary memory flip-flop) and the memory information is reconstructed in the same "non-return to zero" waveform which was originally recorded. Because of the "record-detect-reconstruct" process just described, there is no guarantee that the memory waveform will agree with

the clock-defined pulse times. To eliminate any relative jitter that may be present, the primary memory flip-flop gates clock synchronized signals to a second memory flip-flop which reconstructs the original recorded signal, delayed by a specific number of clock pulses.

The registers used in the transfer system described in the example of digital integration are all segments of the magnetic drum memory. Electronic circuitry needed is thus reduced to a minimum, since the same circuits of the computing section are employed for all registers on a time-sharing basis. The R & Y numbers are recorded on R and Y channels respectively. These channels are divided so that appropriate capacity is allotted to any one set of registers.

The indexing of these registers, recorded sequentially in the memory, is performed by means of counters. Assume the computer under discussion is to represent m integrators (mY registers and mR registers), each of which has n pulses (binary digits) of capacity. By the count in an electronic counter of capacity n, any specific pulse under consideration, of a particular register, is then located in time. The individual registers are similarly accounted for in a counter of capacity m, which keeps track of the integrators. It can be seen that the memory capacity is $m \times n$ pulses, which is the factor determining the spacing between read and record heads.

Interconnections between integrators are made by using a third channel on the drum; this is called the Z or precessing line. The Z channel is used to store the dz output pulses of the integrators as they pass through the computing center. This is accomplished by recording the overflows of the R registers which occur at the Pn, or last pulse time, of an integrator.

The Z line is much shorter than the other memory channels, its length being relative to the number of pulses in one integrator time. By making the delay of this line one pulse time longer or shorter than the number of pulses of one integrator, the pattern recorded will shift by one pulse for each successive integrator time, allowing the recording of new overflows to take the place of obsolete dz information. As long as there are more pulse positions in the Z line than there are integrators, all integrator outputs can be stored in the Z channel and will be available to all integrators.

Corresponding to the R and Y channels there are two address channels Dx and Dy. Proper coding of these channels enables the associated integrator to receive dx and dy information from other integrators. This is done by coincidence circuits. Since the length of the Z line and the timing and ordering of the information supplied to it are known, the time that specific dz information is available for pickup by a given integrator can be predicted. By placing a pulse in the proper position of an address channel, Dx or Dy, desired overflow information or dz outputs of any integrator contained in the Z channel, are available for the digital transfer process as defined by dx and dy inputs of one of the integrators.

The nature of the machine prevents the direct coding of more than one dx pickup for any one integrator; however, more than one dy pickup is possible as long as the number of dy's used for any one integrator does not exceed the capacity designed into the dy section of the computer.

Block Diagram of Computer Operations. The block diagram of figure 2 illustrates an abbreviated serial-memory (magnetic drum) digital differential analyzer, during the computing operation.

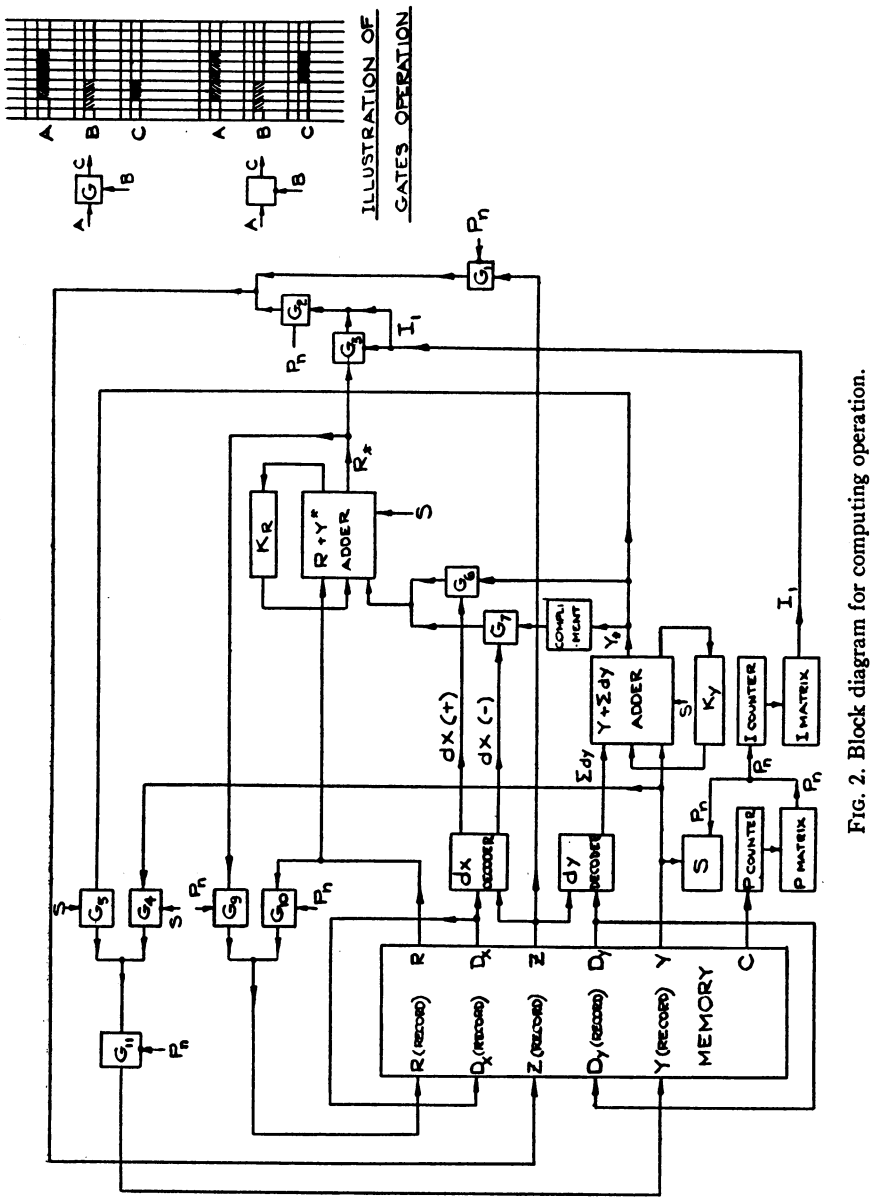

FIG. 2. Block diagram for computing operation.

Consider first the Z channel: the information in this channel is re-recorded through gate $G1$, except at Pn time when this gate closes to block off old information and pass a new overflow from the $R+Y$ adder through gates $G2$ and $G3$. This $G2$-$G3$ system gates an overflow, provided one occurs, with the exception of Pn of word $W1$, at which time $G3$ is blocked and an artificial overflow corresponding to $W1$ is automatically recorded through $G2$ into the memory. In this manner a constant pulse rate dz/dt, which is the rate

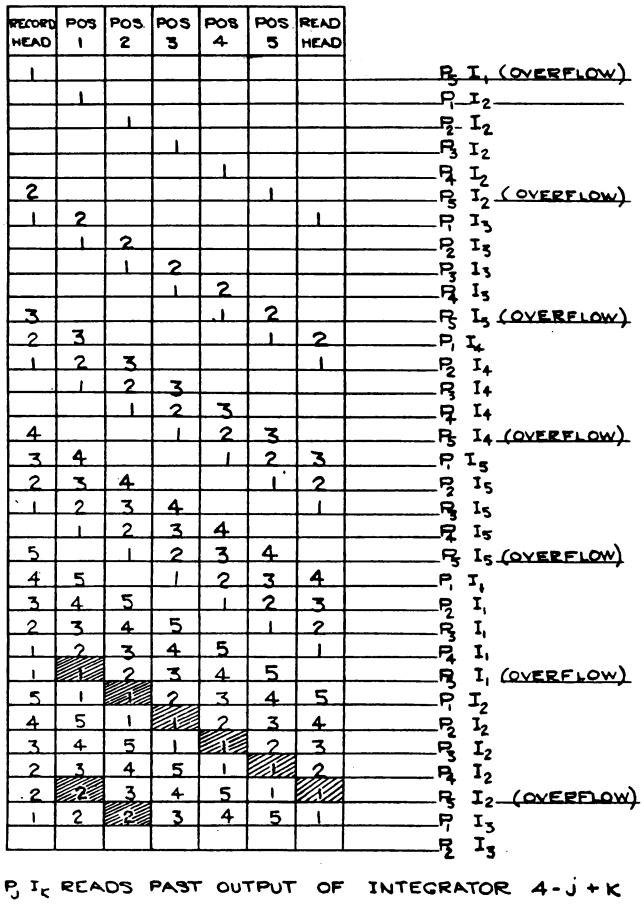

FIG. 3. Precession line for machine of 5 integrators of 5 pulse layers each.

of the independent variable, is generated. The Z information also enters a dy decoder where the Y pickup code extracts the proper pulses from the Z line and accumulates the proper dy increments. This information is then available, as a $\Sigma\, dy$ signal, to the Y portion of an integrator. Timing is such that the proper "connections" reach the right integrators.

The question now arises as to the manner in which the Z information is recorded to distinguish sign. Instead of a plus-zero-minus system, which would be impossible to record in a binary fashion in only one channel, a

plus-minus system is used which has the zero rate biased as alternate ones and zeros (i.e. if a given integrator has successive outputs of 1–0–1–0, etc., its output dz rate is equivalent to zero). This means that any pulse rate from the Z line (representing the continuous outputs of a particular integrator) that has a time average of more ones (recorded overflow) than zeros (absence of a recorded overflow) is positive, while the opposite (more zeros than ones) is a negative rate. The mechanics of this system as it is used in the dy decoder will be explained in a discussion of the number system.

Corresponding to the dy decoder is a dx decoder where the Dx code enables an examination of the Z line to take place, resulting in a signal corresponding to the dz information held in the pulse position of the line being inspected. A dx (+) signal as an output from the decoder corresponds to a one in Z while dx (−) corresponds to a zero. The dx (+) signal controls the addition of Y to R while dx (−) controls subtraction of Y from R.

The address lines never change content during computation and recirculate as shown. These channels are used only to time proper Z line inspection in the decoding sections for integrator interconnections.

The first pulse in the Y section of an integrator, called the start pulse, is a marker which determines the size of the Y number which will be contained in the following portion of the Y number. This pulse is detected by the S flip-flop, which remains in the on state for the rest of the integrator time, turning off at Pn. The numerical portion of Y is added to $\Sigma\, dy$ in the $Y + \Sigma\, dy$ adder resulting in a new Y value, denoted as Y^*. This addition is controlled by the S signal as indicated. Ky is a delay flip-flop holding the carry from one binary digit to the next.

Gate $G4$ passes Y back to the memory as long as the S flip-flop is off. Since the first pulse occurring in Y is the start pulse, this is the only information other than zero passed by $G4$ and it is thus held unchanged in the Y memory during computation. Gate $G5$ passes the new Y, (Y^*), into the Y channel of the memory when S is on. The Y channel then always holds the start pulse and the current $Y + \Sigma\, dy$ sum of the integrators being used in computation. The integrators not used are left blank and recirculate zeros through $G4$.

The $R + Y^*$ adder operates in the same manner as the $Y + \Sigma\, dy$ adder. It has inputs of R, Y^*, and a carry delay flip-flop Kr. However it does not have to be controlled by S since the start pulse is eliminated from Y^* in the $Y + \Sigma\, dy$ adder. Since dx controls the addition of Y^* to R, to the extent that Y may either be added or subtracted, special precaution must be taken. This is accomplished by gates $G6$ and $G7$. If the output of the dx decoder signifies addition, the dx (+) signal opens $G6$ and allows Y^* to be added to R; on the other hand if the dx (−) signal is present, $G7$ is open and the output of a complementing circuit is added to R (this is the same as subtracting Y^* from R).

The output of the $R + Y^*$ adder is denoted by R^*. As previously explained, the overflow pulse of $R + Y^* = R^*$ is the output of the adder at Pn; this is gated into the Z precession loop through $G3$.

As was the case for the start pulse of the Y channel, the information recorded in R at Pn must remain unchanged from one memory cycle to the next. This effect is accomplished by $G9$ and $G10$. The pulse position

Pn in *R* is occupied by what is known as a "sign-reversal pulse." A one in this pulse position reverses the sign of the *dz* output. This operation can be explained as follows: if this pulse position stores a zero a certain pattern of ones and zeros as successive overflows will occur from the $R+Y^*$ adder for a specific integrator.

Consider now the same conditions as above except with a permanent one existing in *Pn* of *R*. The overflow pattern results in an extra one added to the sum at each *Pn* time, thus resulting in the ones and zeros of the sum at this particular pulse time being interchanged, which is a reversal of sign of the output rate.

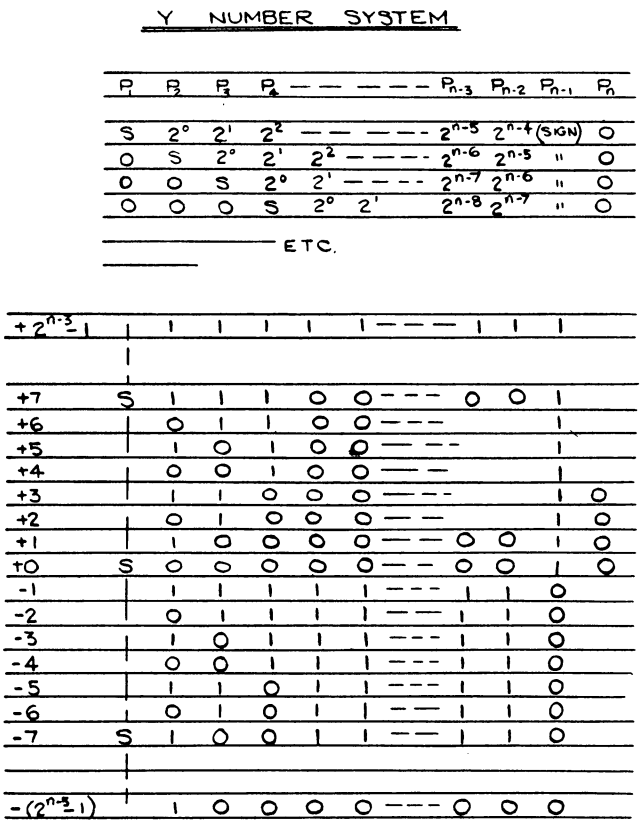

FIG. 4.

***Y* Number System.** The contents of *Y* are shown in figure 4. The first pulse of *Y*, P_1, is the first possible start pulse. The remainder of *Y*, to P_{n-1}, represents the corresponding numerical content of *Y*. In the case where the start pulse is at P_1, P_2 to P_{n-1} is numerical information. P_n is always blank, for this corresponds to the overflow pulse of *R*. P_{n-1} is the sign pulse; a one in this pulse position denotes a positive number, while a zero denotes a negative number. The number system, with the example of the start pulse contained in P_1, is shown in figure 4b. This arrangement allows a *Y* number

capacity of $\pm(2^{n-3} - 1)$. In general the capacity of Y is $\pm(2^{n-2-i} - 1)$ where the start-pulse is placed in P_i. Different arrangements of start-pulse positions are illustrated in figure 4.

The *dy* decoder can be considered as a counter which adds the *dz* overflow pulses in the Z line coincident with the *dy* code channel pulses and subtracts pulses whenever a *dy* code pulse is coincident with no *dz* pulse. Thus at the end of such an accumulation the counter holds the algebraic sum of the 1's and -1's. When this sum (called $\Sigma\, dy$) is sent to the $Y + \Sigma\, dy$ adder, the transfer is done in a serial manner. This transfer is accomplished by a continuous stepping of the counter contents from the first stage Y_1, the signal of the "on plate" of this flip-flop being passed into the adder circuit. The $\Sigma\, dy$ number system and read-out are shown in figure 5 for a

	STAGE 1	STAGE 2	STAGE 3
+3	1	1	0
+2	0	1	0
+1	1	0	0
+0	0	0	0
-1	1	1	1
-2	0	1	1
-3	1	0	1

NUMBER SYSTEM USED IN Σ dy REGISTER.

← STEP

P_{s+1}	1	0	1
P_{s+2}	0	1	1
P_{s+3}	1	1	1
P_{s+4}	1	1	1
ETC.	⋮		

STEPPING PERFORMED BY REGISTER CONTAINING -3 OR Σdy

FIG. 5. $\Sigma\, dy$ register.

computer of 3-stage accuracy. It is the size of this counter-register which determines the *dy* pickup capacity of a given design. It is obvious at this point that the accumulation and stepping cannot be performed simultaneously. For this reason two units are used for this overall operation. The $\Sigma\, dy$ accumulation takes place in one unit, the $\Sigma\, dy$ counter, an integrator time before it is used. It is then transferred into a stepping unit, the $\Sigma\, dy$ register, at the beginning of the next integrator time, and finally stepped into the adder circuit. Figure 6 illustrates the addition of $\Sigma\, dy + Y$.

The Precession Line. To illustrate the operation of the precession line, figure 3 shows a line one pulse time longer than an integrator for a hypothetical machine of 5 integrators, each of 5-pulse capacity. The information

Y= +1		S	1	0	0	0 — — — 0	0	1
Σdy= -3			1	0	1	1 — — — 1	1	1
Ky			1	0	0	0 — — — 0	0	0
Y'= -2			0	1	1	1 — — 1	1	0

FIG. 6. Addition ($Y + \Sigma\, dy$).

at the read and record heads is always the same, except when a new overflow is recorded at the time the new information is introduced to the Z line at the read head. The line is originally clear at the start of computation, picking up its first bit of information at the overflow time of I_1, (P_5I_1). This overflow 1 progresses in the line until at P_5I_2 it is at position 5; at this time 2 is being recorded at the record head. The process builds up until at P_5I_5 all five overflows are recorded. At P_5I_1 (second cycle) a new 1 is recorded replacing the old 1, "shaded position" in actual use. At P_5I_2 the old 1 is replaced by a new 2 which makes the old 2 obsolete. This process continues, making all previous overflow information available to integrators immediately following. The pattern of the Z line can now be defined for any pulse of any integrator. At P_iI_k the information occurring at the read head is the last output of integrator $4 - i + k$. The precession lines used in larger computers are essentially elaborations of this simple example.

Filling and Controls. The discussion of the serial-memory digital differential analyzer has been limited to the computing operation. Memory filling operations are closely related to those of computation in that some of the circuitry of the computer is used for filling.

The essential controls for filling are: channel erasing, channel selection, integrator selection and control of information filled. The erasing control is built into the memory circuitry and consists of a controlled recording, by means of clear switches, of zeros in a channel. The channel selection is accomplished by a switch that controls the logical circuitry at the record end of the computing section. An integrator selector is wired into the integrator counter and matrix in such a manner that a signal is generated corresponding to the integrator time set by this selector. Information is filled into the chosen integrator and channel by keys corresponding to the binary digits, 1 and 0. These keys fill a corresponding one or zero into successive pulse positions P_1 to P_n.

The method of filling successive pulse positions is quite simple and makes use of the Z line. When the machine is idling (neither computing nor filling) all memory channels recirculate, including the precession (Z) line. Before filling, a marker pulse must be placed in the Z line by the operator. This pulse serves as a reference for the pulse position to be filled. When one of the filling buttons is pressed, a circuit, operated by the coincidence of the fill button, integrator selector signal and marker pulse, fills a pulse time in the selected channel with a 1 or 0 corresponding to the button pushed. The marker pulse then shifts by one pulse and is ready for the next digit to be filled. The stepping is done by allowing the Z line to precess once during filling operations at the word time coincident with filling.

CRC 105 Decimal Digital Differential Analyzer. The DDDA (more commonly known as D^{3}A) is the first decimal machine of this type to be designed. The coded-decimal system makes the simple design features of its predecessors applicable and in many instances introduces simplification. This computer will have 60 integrators, each of six-decimal place capacity, plus a position for indication of sign.

External inputs to the DDDA will be stored in the precession line, and unnecessary coding will be eliminated thereby. The inputs will be picked up in the same manner as integrator outputs. Typewriter output on this

machine will allow the contents of up to 12 integrators to be typed out at an interval computed by the machine. This typewriter will eliminate much of the need for auxiliary equipment such as graph plotters, etc.

The computer will be able internally to limit the maximum and minimum of functions, which is of great advantage in dealing with non-linearities occurring in electronics and servo problems.

Means of storage of initial conditions during computation will eliminate the tedious refilling ordinarily necessary in repetitive problems, where families of solutions or experimental solutions are made.

The serial-memory digital differential analyzer was co-invented by D. E. ECKDAHL, R. E. SPRAGUE, H. H. SARKISSIAN, C. L. ISBORN, A. E. WOLFE, W. F. COLLISON, and F. G. STEELE.

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DISCUSSIONS

The Adventures of a Blunder

Those who regularly code for fast electronic computers will have learned from bitter experience that a large fraction of the time spent in preparing calculations for the machine is taken up in removing the blunders that have been made in drawing up the programme. With the aid of common sense and checking subroutines the majority of mistakes are quickly found and rectified. Some errors, however, are sufficiently obscure to escape detection for a surprisingly long time. The blunder which is the excuse for this note falls in this class and to the writers' knowledge was responsible for only one arithmetical error in its whole career! How many other errors of a similarly obscure character are still at large in the EDSAC library can only be conjectured but one at least has been reported to us by Dr. A. VAN WIJNGAARDEN.

The blunder arose from the misuse of a subroutine for calculating the square roots of numbers in floating decimal form. Numbers in this form are expressed as $a \cdot 10^p$, where p is an integer. Calculations are carried out using a "floating decimal accumulator," that is, a pair of storage locations set aside for holding a number which is being operated on in floating decimal form. Before being transferred from the floating decimal accumulator to another part of the store, each number is standardised so that $1 < |a| \leq 10$. In the floating decimal accumulator itself, $|a|$ may lie outside this range (the representation being not unique). Thus in the multiplication of two numbers each in standard form, the two numerical parts are multiplied yielding a number in the range $1 < |a| \leq 100$, and this is left in the floating decimal accumulator as it stands. Similarly, addition of two standard numbers may leave the numerical part anywhere in the range $0 \leq |a| \leq 20$, the exponent being that of the larger component.

A programme was prepared which involved finding the modulus of a complex number $X + iY$. A square root subroutine was used for finding the square root of the quantity $X^2 + Y^2$. This square root subroutine causes a number held in the floating decimal accumulator in standard form to be replaced by its square root. However, the requirement that the argument should be in standard form was overlooked in the preparation of the sub-

routine. Strangely enough the programme passed lengthy tests successfully and the blunder was only discovered when the coding of a similar problem led to the investigation of this particular detail. Further investigations showed that the chance of the blunder producing an error was indeed small, about 1 in 256. The explanation is given below.

First it was found that the square root subroutine would, in fact, function correctly if $|a| < 16$, or if p was even and $|a| < 160$, and it happened that this restriction was met by nearly every case encountered in the programme. The reason for this is as follows. Let the complex number be $X + iY$, where X is expressed as $x \cdot 10^q$ and Y as $y \cdot 10^r$. First, X^2 was formed and transferred to the store, being thus standardised as, say, $z \cdot 10^s$, which could be either $x^2 \cdot 10^{2q}$ or $(x^2/10) \cdot 10^{2q+1}$. Then Y^2 was formed in the floating decimal accumulator and X^2 added to it, and the square root subroutine was called in. At this stage we can distinguish two cases:

(i) $s \leq 2r$. The exponent in the floating decimal accumulator is $2r$, and $X^2 + Y^2$ appears as $(y^2 + z \cdot 10^{s-2r}) \cdot 10^{2r}$. The exponent is even and the numerical part does not exceed 110; hence the subroutine works correctly;

(ii) $s > 2r$. The exponent is s and the numerical part is $(y^2 \cdot 10^{2r-s} + z)10^s$. If s is odd, $s = 2q + 1$ and the numerical part may be as high as 16 only if $q = r$, in which case the restriction may be violated. The subroutine works correctly unless $q = r$, or $x^2 + y^2 \geq 160$. The likelihood of this violation can be roughly estimated by assuming a logarithmic probability distribution of the modulus and a rectangular distribution of the argument. With this assumption the probability of an error is .0039. The error is thus rare enough to escape notice in all but exhaustive tests.

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The contents are as follows:

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2. The CADAC
3. The SEAC
4. The SWAC
5. Whirlwind I
6. Moore School Automatic Computer (MSAC)
7. The Burroughs Laboratory Computer
8. Naval Proving Ground Calculators
9. Aberdeen Proving Ground Computers

The ENIAC
The ORDVAC
The EDVAC

Special Purpose Computer

1. MADDIDA

Data Processing and Conversion Equipment

1. The Charactron
2. Wallind-Pierce Equipment
3. Aurex Magnetic Wire Storage
4. CRC Ferro-Resonant Flip-Flop

2. ANON., "New instruments," *Rev. Sci. Instruments*, v. 22, July 1951, p. 544–545.

High-speed analog to digital converter announced by Arthur D. Little, Inc., Cambridge 42, Mass., takes an input voltage varying from 0 to 50 volts, samples it up to 50,000 times a second, and converts the readings to 7-digit binary numbers expressed as pulses on seven output leads.

Analog-digital converter announced by Glenisco, Inc., 2233 Federal Avenue, Los Angeles 64, Calif., counts shaft rotations in the decimal system to a least count of 0.1 revolution by means of solenoid actuated quantizers.

R. D. ELBOURN

NBS Electronic Computers

3. STUART R. BRINKLEY, JR., "Evaluation of performance factors of fuel-oxidant mixtures," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2471–2475.

This paper concerns itself with the solution of equations of condition for thermodynamic equilibrium in multicomponent gas mixtures. The resulting non-linear simultaneous equations are solved with the help of the Newton-Raphson method. The calculations were made on the IBM Card-Programmed Calculator,[1] using the general purpose board on which the author collaborated.

M. ABRAMOWITZ

NBSCL

[1] STUART R. BRINKLEY, JR., G. L. WAGNER, & R. W. SMITH, JR., "General purpose ten-digit arithmetic on the IBM Card-Programmed Electronic Calculator," *Proceedings of Industrial Computation Seminar*. New York, IBM, 1950.

4. H. W. BRAUGH, W. G. SCHLINGER & B. H. SAGE, "Evaluation of equation of state constants with digital computers," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2442–2446.

In fitting the Benedict equation of state for the lighter hydrocarbons to experimental data, a technique of least squares is employed to evaluate the constants. The equations involved are complicated by a series of exponential terms and are arranged for solution by automatic digital computing machines. Tabular results for the Benedict equations for propane and methane, obtained with an IBM Type 604 Calculator, are presented.

J. WEGSTEIN

NBSCL

5. J. W. DONNELL & R. W. DRAPER, "Absorption calculations by punch card calculators," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2449–2453.

A procedure is given to eliminate the trial and error methods in accurate calculations made to determine the number of absorber trays and amount of absorber medium necessary to yield a given absorption. The systems of simultaneous equations obtained from the conditions of material balance and heat balance are solved by an iteration technique. Starting with preliminary estimates the iteration is carried through a number of cycles until convergence is obtained. The calculations are made on the IBM 602 Calculating Punch and are so routinized that no judgment is necessary in the successive steps of the procedure.

M. ABRAMOWITZ

NBSCL

6. R. M. GOODMAN, "A digital computer timing unit," I.R.E. *Proc.*, v. 39, Sept. 1951, p. 1051–1054.

The EDVAC, a synchronous serial computer, requires a set of 48 timing pulses, each of which occurs at a particular pulse time within the 48-pulse minor cycle. These come from a six-by-eight array of gates. Rows are governed by the tap points on a six pulse-time delay line which accepts every sixth clock pulse, and columns are governed by eight flip-flops which are triggered by the last timing pulse from each column.

R. D. ELBOURN

NBS Electronic Computers

7. GILBERT W. KING, "Monte Carlo method for solving diffusion problems," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2475–2478.

This article is a brief survey of some problems that have been handled by the Monte Carlo technique. It is pointed out that it has been customary but not necessary in solving problems in mathematical physics to formulate them as differential equations to be solved. Using Monte Carlo methods, highly realistic models representing very complex problems in classical physics or chemistry may be handled without going through the abstraction of the differential equation. The power and simplicity of the Monte Carlo method, when large scale computing facilities are available, is emphasized, and illustrations are given for several types of diffusion problems.

J. H. LEVIN

NBSCL

8. FREDERICK J. MARTIN & MORRIS YACHTER, "Calculation of equilibrium gas compositions," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2446–2449.

The authors consider a set of non-linear, algebraic equations:

$$\sum_{j=1}^{n} a_{ij}x_j = f_i(x_1, x_2, \cdots, x_n), \qquad i = 1, 2, \cdots, n$$

which we will write

$$Ax = f(x). \tag{1}$$

If x is the solution, and $\bar{x}$ is an initial guess to the solution, the authors then wish to solve for the error

$$\Delta x = x - \bar{x} \tag{2}$$

by means of the following expansion:

$$A(\bar{x} + \Delta x) \cong f(\bar{x}) + J(\bar{x})\,\Delta x$$

or

$$[A - J(\bar{x})]\,\Delta x \cong f(\bar{x}) - A\bar{x} \tag{3}$$

where $J(\bar{x})$ is the Jacobian matrix evaluated at $\bar{x}$.

Equation (3) is a linear equation for Δx which is easily solved and the solution Δx is then substituted in (2) to yield the next approximation to x. The process is then repeated until the iteration converges.

As a labor saving device, the authors suggest computing $J(\bar{x})$ just once and using the same matrix $A - J(\bar{x})$ in (3) for all further iterations.

LEON NEMEREVER

NBSCL

9. ASCHER OPLER & ROBERT G. HEITZ, "Punched-card calculation of six-component distillation," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2465–2471.

A procedure is given for the calculation of the plate composition of six-component continuous distillation in thermal balance. The equations resulting from the conditions of material balance and heat balance are solved by trial and error. The computations were made with the IBM 602A Calculating Punch.

M. ABRAMOWITZ

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10. ARTHUR ROSE, R. CURTIS JOHNSON, & THEODORE J. WILLIAMS, "Stepwise plate-to-plate computation of batch distillation curves," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2459–2464.

The application of the IBM Card-Programmed Calculator to the prediction of distillation operations is discussed. The problem is discussed for the case of non-ideal conditions such as carrying relative volatility, non-adiabaticity, varying plate holdup, beating effects, and condenser holdup. Comparison of the computed results with experiment is also made.

M. ABRAMOWITZ

11. ARTHUR ROSE, R. J. LOMBARDO, & THEODORE J. WILLIAMS, "Selective adsorption computations with digital computers," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2454–2459.

The authors discuss the approximate solution of the problem of adsorption in liquids by considering the relations obtained from conditions of

successive material balance in different types of mixtures. The resulting system of equations is solved recursively on the IBM Card-Programmed Calculator using a general purpose board.

M. ABRAMOWITZ

12. ARTHUR ROSE, THEODORE J. WILLIAMS, & HARRY A. KAHN, "Digital computers for trial and error calculations of distillation design," *Industrial and Engineering Chemistry*, v. 43, Nov. 1951, p. 2502–2506.

This paper discusses the application of the IBM Card-Programmed Calculator to distillation problems involving trial and error techniques for solution. Assuming certain basic conditions for the distillation, the authors determine the remaining product compositions employing the relations for material balance. A description of the machine procedure is given in some detail, and the results are described for the determination of the reflex ratio under the assumption of constant relative volatility. The extensions to non-constant relative volatility and nonadiabatic operation are also discussed.

M. ABRAMOWITZ

NEWS

Joint AIEE-IRE Computer Conference Committee.—This committee, with the participation of the Association for Computing Machinery, held a meeting in Philadelphia on December 10, 11, and 12, 1951. Some 900 persons attended the meeting. The program of the conference was the following:

Monday, December 10

Morning Session	J. G. BRAINERD, Moore School of Engineering, University of Pennsylvania, *Chairman*
Keynote Address	W. H. MACWILLIAMS, Bell Telephone Laboratories
The UNIVAC System	J. P. ECKERT, JR., J. R. WEINER, H. F. WELSH, and H. F. MITCHELL, JR., Eckert-Mauchly Computer Corporation, Division of Remington-Rand, Inc.
Performance of the Census UNIVAC System	J. L. MCPHERSON, Bureau of the Census, and S. N. ALEXANDER, National Bureau of Standards
Afternoon Session	I. TRAVIS, Burroughs Adding Machine Company, *Chairman*
The Burroughs Laboratory Computer	G. R. HOBERG, Burroughs Adding Machine Company
Inspection Trips	Eckert-Mauchly Division of Remington-Rand, Technitrol Engineering Company, Burroughs Research Division, and Moore School of Electrical Engineering
Evening Session	H. E. TOMPKINS, Burroughs Adding Machine Company, *Chairman*
The Significance of Electronic Computers to Science and Management	S. N. ALEXANDER, National Bureau of Standards

Tuesday, December 11

Morning Session	C. V. L. SMITH, Office of Naval Research, *Chairman*
IBM Card-Prógrammed Calculator	J. W. SHELDON and L. TATUM, International Business Machines Corporation
The ORDVAC	R. E. MEAGHER and J. P. NASH, University of Illinois
Afternoon Session	Dr. MINA REES, Office of Naval Research, *Chairman*
The ERA 1101 Computer	F. C. MULLANEY, Engineering Research Associates
The Operation of the Mark III Calculator	G. E. POORTE, U. S. Naval Proving Grounds, Dahlgren, Virginia
The University of Manchester Computing Machine	T. KILBURN, University of Manchester, England, and B. W. POLLARD, Ferranti, Ltd.

Wednesday, December 12

Morning Session	J. M. COOMBS, Engineering Research Associates, *Chairman*
Whirlwind I Computer	R. R. EVERETT and N. H. TAYLOR, Massachusetts Institute of Technology
The EDSAC Computer	M. V. WILKES, University of Cambridge, England
The National Bureau of Standards Eastern Automatic Computer (SEAC)	S. N. ALEXANDER and R. J. SLUTZ, National Bureau of Standards
Afternoon Session	A. E. SAMUEL, International Business Machines Corp., *Chairman*
The Transistor as a Computer Component	J. FELKER, Bell Telephone Laboratories
Summary and Forecast	J. W. FORRESTER, Massachusetts Institute of Technology

Centre International de Calcul Mécanique.—At a conference held in Paris in November, 1951, the UNESCO voted to establish the Centre in Rome, Italy. This choice was influenced, no doubt, by the fact that Rome is the seat of the Istituto Nazionale per le Applicazioni del Calcolo, headed by M. PICONE. A quarter of a century ago, Professor Picone established the Istituto di Calcolo in Naples. In 1932 it was moved to Rome, under its present name, and is located in the same building as the Italian National Council of Research. This building will be considerably enlarged to accommodate the Centre. It will contain at least one high-speed electronic calculating machine and will be staffed by specialists recruited from all participating nations. The Centre's yearly expenditure is expected to be around $130,000, which will be met by all the participating nations (about 20 in number) as well as by the Centre's earnings from services rendered to private organizations in any country requesting them. On the other hand, these services will be available without charge to government scientists of the nations.

A number of Italian scholars are already in the United States engaged in an extensive survey of electronic computation techniques and the engineering principles involved in the construction of high-speed calculators. Drs. DINO DAINELLI and ENZO APARO, members of Professor Picone's Istituto, have been at the NBSCL for the past three months and have computed several important mathematical functions on the SEAC. They are planning an extended stay at the Harvard Computation Laboratory also, where they will join GUILIO RODIÑO. The latter, an electronic engineer, replaced his colleague, MICHELE CANEPA, who returned to Italy after a year's study of Harvard's high-speed computers.

The first post as American observer at the Centre is held by Dr. HERMAN GOLDSTINE of the Institute for Advanced Study, Princeton University.

UNIVAC Acceptance Tests.—On February 4–5, 1952, the second UNIVAC, constructed by the Eckert-Mauchly Division of Remington Rand under NBS contract for the Office of the Air Comptroller, USAF, passed a magnetic tape reading and writing test which was the final test for its acceptance. The machine is now being moved from the factory in Philadelphia to the Pentagon Building in Washington, D. C., where its primary activity will be computing logistic programs.

In this test UNIVAC read over 142 million decimal digits from magnetic tapes and wrote over 85 million on tapes in eight hours net running time and two hours down time. It ran without error or stoppage through 23 out of 32 fifteen-minute test units. In the other 9 test units automatic checking circuits stopped the machine for 15 tape reading errors, for two malfunctions of tape driving mechanisms, for two tape defects, and for one tube failure in the computer. No errors escaped the automatic checking circuits.

The same general test of computational ability that was given the first UNIVAC was also given to this machine. (See *MTAC*, v. 5, p. 176–7.) During the 19 twenty-minute test units, the only malfunctions were three tape reading errors which were detected by automatic checking circuits.

The test of the Uniprinter required it to read from magnetic tape and to type 144,000 characters among which occurred every typewriter symbol. This took four hours and fifty-four minutes running time plus nineteen minutes down time. Checking circuits stopped the printer six times, apparently because it picked up spurious pulses in the spaces between blocks of data on the tape. No errors were found in the copy.

The Unityper test required 54,000 characters of instruction codes to be typed onto magnetic tapes and these to be readable by UNIVAC and by Uniprinter. Net typing time was 3½ hours. UNIVAC read all the tapes correctly, but Unityper omitted characters at three points because tape slippage on Unityper had caused them to be recorded too closely together.

In the Bureau of the Census's year of experience with the first UNIVAC the computer has been remarkably reliable except for rather frequent tape reading error; therefore the tape reading and writing test for the second UNIVAC was revised to require nearly five times as much reading. For this reason the similarity in performance of the first and second UNIVACS in their tests really indicate noteworthy improvement in this respect.

OTHER AIDS TO COMPUTATION

Bibliography Z–XIX

13. Anon., "Aircraft and flight-control-system analog," *Instruments*, v. 23, 1950, p. 568, 570.

A description with three pictures of the M. I. T. Flight Simulator constructed under the supervision of A. C. Hall. This device consists of a continuous computer and a three gimbal flight table positioned by hydraulic servos.

F. J. M.

14. Anon., "Analog computer," *Instruments*, v. 24, 1951, p. 772, one photograph.

This article describes a differential analyzer suitable for solving systems of differential equations with constant coefficients constructed for M. I. T. by a Boston firm. The device is electrical, set up by means of patch cords, and can handle six equations in six unknowns. It "is not a commercial product."

F. J. M.