103[L].—SIDNEY JOHNSTON, *Tables of Sievert's Integral*, manuscript in possession of the author, photograph copy at NBSCL.

This is a table of the function

$$\int_0^x \exp(-A \sec t)dt$$

for $A = 0(.5)10$ and $x = 0(\pi/180)\pi/2$. Values are given mostly to 5S. Explicit tabulation is not made beyond a value of x where the integral remains unchanged to 5S.

104[V].—SIDNEY KAPLAN, *Tables of Velocity Functions Characterizing Flows Formed by Jets from Orifices*. U. S. Naval Ordnance Laboratory Memorandum, 87 p. Available only to government agencies and contractors.

The basic mathematics governing the flow of incompressible fluids has been known for many years. Because a great amount of tedious computation is necessary, flows for only a few isolated cases have been calculated in the past. At the suggestion of G. BIRKHOFF,[1] the Naval Ordnance Laboratory has calculated for the first time the flow patterns of an incompressible fluid from an orifice for four different angles of aperture: $\alpha = 0°, 15°, 45°$, and $90°$. In all, more than 2,000 points were calculated.

The governing equations are

$$W = U + iV = \ln(\zeta) - \ln(\zeta^2 - 2C\zeta + 1) \tag{1}$$

$$Z = x + iy = z' + iSz'' \tag{2}$$

$$\zeta = \xi + i\eta, \qquad |\zeta| \leqslant 1, \qquad 0 \leqslant \arg\zeta \leqslant \pi \tag{3}$$

$$Z' = -\zeta^{-1} + C(W + \ln\zeta) \tag{4}$$

$$Z'' = \ln\left[\frac{\zeta - \exp(i\alpha)}{\zeta - \exp(-i\alpha)}\right], \qquad \alpha < \arg Z'' \leqslant \pi + \alpha \tag{5}$$

where $S = \sin\alpha$, $C = \cos\alpha$, and values for α, U, V are as follows.

α	Range in U	Range in V	Number of Cases
0	$-2.8(.2)2$	$0(\pi/20)\pi$	525
$\pi/12$	$-2.4(.2)3.2$	$0(\pi/20)\pi$	609
$\pi/4$	$-2.4(.2)1.6$	$0(\pi/20)\pi$	441
$\pi/2$	$-2.4(.1)1.6$	$0(\pi/20)\pi/2$	451

x and y are given to 4D and ξ and η are given to 5D. In each case the error is less than a half a unit in last place.

[1] G. BIRKHOFF, & E. ZARANTANELLO, *Jets, Wakes and Cavities*, soon to be published.

AUTOMATIC COMPUTING MACHINERY

Edited by the Staff of the Machine Development Laboratory of the National Bureau of Standards. Correspondence regarding the Section should be directed to Dr. E. W. CANNON, 225 Far West Building, National Bureau of Standards, Washington 25, D. C.

TECHNICAL DEVELOPMENTS

The Incorporation of Subroutines into a Complete Problem on the NBS Eastern Automatic Computer

The construction of a modest-scale automatically-sequenced electronic digital computer at the National Bureau of Standards is nearing completion. This computer, called the NBS Eastern Automatic Computer (SEAC), is expected to be a useful tool both for numerical computation and for research in numerical analysis. In order to facilitate the exploitation of the SEAC, the Machine Development Laboratory of the Bureau has planned in advance key instruction routines for use on the machine. Groups of these instruction routines will be incorporated as subroutines in instruction programs governing the solution of complete problems. It is the purpose of this paper to show how subroutines prepared in advance of problem solution, selected from a library of permanent subroutines, will be properly inserted by the computer in the instruction program relevant to a problem at hand.

In order to follow this program it will be necessary to understand the principal features of the logical design of the SEAC.

1. Memory.—The present routine is written to fit the initial model of the machine which has 64 acoustic lines, or tanks, each line storing eight "words." A word consists of 48 binary digit positions, of which 45 are used to represent either a number or a four-address command, and the remaining three provide spacing between words. A number, N, of 44 binary digits followed by a sign digit, is stored as an absolute value with the proper sign attached. A plus sign is represented by "0" and a minus sign by "1." The binary point of the number is located between the second and third positions from the left so that $|N| < 4$.

In the operation representation, 10 binary positions are apportioned to each of four addresses, or memory locations. As there are only 512 memory locations in the initial model, nine binary digits are sufficient to specify any address (six digits to indicate the tank number and three digits to indicate the word within that tank). The first binary digit from the left of any address will always be zero and therefore will not be indicated here. The remaining nine binary digits will be represented by three octal digits. In addition, four binary digits represent, in coded form, the operations to be performed, designated herein by capital letters. The 45th digit from the left is again a sign indicator.

The following important feature of the acoustic-line memory should be kept in mind: information sent to an address will replace the previous content of that address.

2. Command Code.—In Table I under the headings of each of the four addresses α, β, γ, and δ the items which are located therein are listed. An address enclosed in parentheses indicates the content of the corresponding memory location; the address of the next command is abbreviated as "n.c."

The 45th binary digit from the left in a command is normally a zero (i.e., a plus sign); when a minus sign is coded in that position, the machine

TABLE I

Operation	α	β	γ	δ	Operation Symbol	Result of Operation
Addition	Augend	Addend	Sum	n.c.	A	$(\gamma) = (\alpha) + (\beta)$
Subtraction	Minuend	Subtrahend	Difference	n.c.	S	$(\gamma) = (\alpha) - (\beta)$
Multiplication (High-order)	Multiplicand	Multiplier	High-order Product	n.c.	M	(γ) = the more significant half of $(\alpha)(\beta)$
Multiplication (Low-order)	Multiplicand	Multiplier	Low-order Product	n.c.	N	(γ) = the less significant half of $(\alpha)(\beta)$
Multiplication (Rounded)	Multiplicand	Multiplier	Rounded Product	n.c.	R	(γ) = the more significant half of $(\alpha)(\beta)$ increased by the first digit of the less significant half of the product
Division	Divisor	Dividend	Quotient	n.c.	D	$(\gamma) = (\beta)/(\alpha)$, unrounded
Logical Transfer	Extractee	Extractor	Altered Number	n.c.	L	Digits in (γ) which correspond to 1's in (β) are replaced by corresponding digits of (α)
Algebraic Comparison	1st Comparand	2nd Comparand	n.c. or	n.c.	C	(γ) = n.c., if $(\alpha) < (\beta)$ (δ) = n.c., if $(\alpha) \geq (\beta)$
Absolute Value Comparison	1st Comparand	2nd Comparand	n.c. or	n.c.	K	(γ) = n.c., if $\lvert(\alpha)\rvert < \lvert(\beta)\rvert$ (δ) = n.c., if $\lvert(\alpha)\rvert \geq \lvert(\beta)\rvert$
Input Order	Any Number	Odd Number	Word from Input	n.c.	T	(γ) = next word from Input medium
Input Order	Any Number	Even Number	Word from Input	n.c.	T	(γ) to $(\gamma + 7)$ = next 8 words from Input medium
Output Order	Any Number	Odd Number	Word to be Recorded	n.c.	P	(γ) = next word on Output medium
Output Order	Any Number	Even Number	Word to be Recorded	n.c.	P	(γ) to $(\gamma + 7)$ = next 8 words on Output medium

will stop automatically after executing the indicated operation. Commands can be manipulated in the arithmetic unit of the machine, since, to this unit, they are indistinguishable from numbers.

3. Timing.—A minor cycle, the time needed for one word to pass a given point in the machine, is equal to 48 microseconds. The time consumed for a given operation, located at address ϵ, can be obtained from the following formulae (where an underscored symbol represents the last octal digit of the indicated address):

1. For operations A, S, and L, $t = (\underline{\epsilon} - \underline{\beta}) + (\underline{\beta} - \underline{\alpha}) + (\underline{\alpha} - \underline{\gamma}) + (\underline{\gamma} - \underline{\delta})$, where 8 minor cycles must be added to each difference which is algebraically less than $+1$.
2. For operations M, N, R, and D, the above sum must be increased by 40 minor cycles if $(\underline{\alpha} - \underline{\gamma}) \geq 5$; otherwise, the sum must be increased by 48 minor cycles.
3. For operations C and K, two timings are possible depending on the result of the comparison; the number of minor cycles is given by $(\underline{\epsilon} - \underline{\beta}) + (\underline{\beta} - \underline{\alpha}) + (\underline{\alpha} - \underline{\gamma})$, if $(\alpha) < (\beta)$, or $(\underline{\epsilon} - \underline{\beta}) + (\underline{\beta} - \underline{\alpha}) + (\underline{\alpha} - \underline{\delta})$, if $(\alpha) \geq (\beta)$. In this case, 8 minor cycles must be added to the first two differences whenever their value is less than $+1$ and to the third difference whenever its value is less than $+2$.

The following table indicates the range of execution time for each command:

Operation	Minimum Time minor cycles	microsec.	Maximum Time minor cycles	microsec.
C, K	4	192	25	1200
A, S, L	4	192	32	1536
M, N, R, D	48	2304	76	3648
T, P	About 2 seconds per word, at present			

4. Modification of Subroutines.—In 1947, SAMUEL LUBKIN considered the problem of modifying subroutines which were to be used in a given problem to fit the available machine storage. He proposed the use of a Base Number Command to simplify the task of adapting any subroutine to its position in the memory. GOLDSTINE & VON NEUMANN[1] have reported on the programming of such adaptation using the codes of the Institute for Advanced Study machine. A similar routine prepared for use on the SEAC is presented herein. Because of the restricted storage capacity of this machine, an effort has been made to pack frequently-used routines in the internal memory as economically as possible. The present routine, in which the assumption is made that n subroutines are to be incorporated within the given program, occupies only $17 + n$ cells. This number does not include, however, four temporary storage cells and the storage for nine constants which belong to a common pool (as explained in the next section).

A general explanation of the method used in the modification of subroutines for insertion in main instruction routines will perhaps be helpful to the reader. Each permanent subroutine is coded as though its first word were located at the address 0 100 000 000 (i.e., the binary equivalent of the octal address 400). All addresses in the subroutine which require modification, as introduced into the computer, are greater than 400. Thus, there will be a "1" present in the second position of every address which must be modified and a zero in the corresponding position of all other addresses which are less than 400.

In the present program, each of the required group of subroutines is inserted into the memory in the final locations it is to occupy. The modifying routine begins at position 050. All addresses of 400 or above contained within the subroutine are modified to fit the actual location of the subroutine in the memory. In substance, the four digits corresponding to the second digit from the left of each address within such words of the subroutine as need modification are extracted. The resulting number is multiplied by d, which represents the difference between the address occupied by the first word of the subroutine under consideration and the number 400 at which address this word was originally coded. The resulting product is added to the original word, and the addresses contained therein are thereby properly modified.

Consider a specific example illustrating this procedure. As stated above the addresses will be written in octal form, although they are stored in binary form. Suppose the following subroutine operation, originally coded at address 400, is placed in the memory at address 070:

Cell No.	α	β	γ	δ	Operation
070	401	046	401	415	A

In order to modify (070), subtract 400 from 070 octally with the result, $d = -310$. Next, extract the second binary digit from the left of each address giving a "1" in the case of α, γ, and δ and a "0" in the case of β. Multiply each extracted digit by $d = -310$, giving -310 in the α, γ, and δ positions of a memory cell and 000 in the β position, and add the result octally to (070). The modified operation is as follows:

Cell No.	α	β	γ	δ	Operation
070	071	046	071	105	A

After all the subroutines in a program are modified, the memory cells occupied by the modifying routine are available for other uses.

5. Conventions Used in Coding.—Before actually presenting the program, it will be necessary to explain some of the conventions used in the coding of this routine. An address enclosed within brackets is used to indicate the fact that the content of that storage location will vary. Braces are used in the ordinary algebraic sense.

The first two memory tanks (i.e., memory locations 000 through 017) are retained for temporary storage in the modification routine; cell 007 contains the instruction to be executed immediately after the routine is completed. Positions 020 through 047 serve as a common pool of frequently-used constants, which all subroutines employ. Of this pool, the present routine makes use of the following constants:

Memory Cell	Content
020	+ Zero
023	400 (in binary form) occupying the α space, zeros occupying the remaining binary positions
027	the number 2^{-8}, representing a unit in the last position of α
031	the number 2^{-22}
034	the number 2^{-28}, representing a unit in the last position of γ
041	the number 2^{-10}
042	$2^{2} - 2^{-8}$, representing 10 units occupying the α space
044	$2^{-18} - 2^{-28}$, representing 10 units occupying the γ space
047	Zero (at the start of the routine only)

The following notations will be used in the program:

Notation	Significance
a_{ij}	the address at which the j-th word of the i-th subroutine is located, where $i = 1, 2, 3, \cdots n$ and $j = 1, 2, 3, \cdots b_i$
b_i	the number of words to be modified in the i-th subroutine
$\overline{w}_{ij}$	the content of cell a_{ij} before modification
w_{ij}	the content of cell a_{ij} after modification
s_k	the binary digit of $\overline{w}_{ij}$ in position k from the left, where $k = 1, 2, 3, \cdots 45$

PROGRAM

Cell No.	α	β	γ	δ	Operation	No. of minor cycles	Result of Operation
050	070	044	055	062	L	14	(055) = 010 013 a_{i1} 061 A
062	070	031	012	063	N	55	(012) = $2^{-18}a_{i1}$ (see footnote 2)
063	041	012	012	067	D	52	(012) = $2^{-8}a_{i1}$
067	012	042	051	064	L	19	(051) = a_{i1} 020 010 066 A
064	012	023	012	051	S	11	(012) = $\{a_{i1} - 400\}2^{-8} = d$
051	[a_{ij}]	020	010	066	A	12	(010) = $\overline{w}_{ij}$

Cell No.	α	β	γ	δ	Operation	No. of minor cycles	Result of Operation
066	010	065	047	054	L	10	$(047) = s_2 2^0 + s_{12}2^{-10} + s_{22}2^{-20} + s_{32}2^{-30} = t$
054	047	012	013	055	M	63	$(013) = td = c$, correction
055	010	013	$[a_{ij}]$	061	A	14	$(a_{ij}) = \bar{w}_{ij} + c = w_{ij}$
061	051	070	052 / 056		K	15/11	Test as to whether b_i modifications have been made.
052	027	051	051	060	A	10	If b_i modifications have not been made, (051) and (055) are stepped up.
060	034	055	055	051	A	15	
056	[071]	020	070	057	A	16	All b_i modifications have been made; $(070) = [\{a_{i1} + b_i - 1\}2^{-8} + a_{i1}2^{-28}]$, where $i = 2, 3, \cdots, (n+1)$.
057	027	056	056	053	A	12	(056) is stepped up.
053	020	070	050 / 007		K	19/20	Test as to whether n subroutines have been modified.

Temporary and Constant Storage

065	$2^0 + 2^{-10} + 2^{-20} + 2^{-30}$
070	$\{a_{11} + b_1 - 1\}2^{-8} + a_{11}2^{-28}$; $[\{a_{i1} + b_i - 1\}2^{-8} + a_{i1}2^{-28}]$
071	$\{a_{21} + b_2 - 1\}2^{-8} + a_{21}2^{-28}$
. . .	. . . .
$067 + n$	$\{a_{n1} + b_n - 1\}2^{-8} + a_{n1}2^{-28}$
$070 + n$	Zero

In this program the commands are arranged in logical sequence. On the input medium, they would be arranged in numerical order of addresses of the memory cells containing them. The time consumed for each instruction to be modified is 6.5 milliseconds.

MDL Staff

NBSMDL

[1] H. H. GOLDSTINE, J. VON NEUMANN, *Planning and Coding of Problems for an Electronic Computing Instrument*, Part II, v. 3, Institute for Advanced Study, Princeton, N. J., 1948 [*MTAC*, v. 3, p. 541–542].

[2] Because the first two digits from the left in the result of low order multiplication on the SEAC are always zero, two instructions are required to put a_{i1} into the α position of memory cell 012.

DISCUSSIONS

A Note on "Is" and "Might Be" in Computers

Recent press reports have aired the disagreement between the "brain" and the "antibrain" factions in the computer fraternity. The term "brain" is a bit fanciful and perhaps smells slightly like commercial advertising; however, I feel that some of the stories given to the press have been more definitely misleading. I would like to enter a plea for careful distinction between facts and fancies by scientific people who write and speak for the general public.

A specialist in one field must be particularly careful in talking to the public about matters not in his own field of specialization. A careless or exaggerated remark made to experts in a field will do little harm because

the audience will make suitable allowance for "embroidery," but a similar remark made to the general public may be taken seriously and may lead to real misunderstanding.

At the present critical period in the development of science, when scientists are being forced somewhat reluctantly to take a hand in international affairs, there is much loose talk on the part of those who were formerly in undisputed control. Instead of excusing similar inaccuracies on the part of scientists, this seems to me to emphasize our responsibility to the public to present fair, accurate, and dependable statements.

This note is frankly an appeal to those who issue frequent statements to the public press, to distinguish carefully between imagination and fact—between what "might be" and what "is." I fear that these categories have been confused on several occasions.

The analogy between computers and the brain or nervous system, for example, has been a useful aid to invention and, when properly qualified, to an understanding of the workings of a computer. Invention, as I imagine it, consists of selecting out of many random combinations of ideas some that serve a useful purpose. Any device, no matter how devoid of logic, that helps to form useful combinations should be accepted thankfully. In this role, by suggesting what might be, the "brain" analogy had been useful to me and probably to others, particularly in the formative period of computer development. Once a combination of ideas has been formed, however, it must stand on its own logical feet; one must then be careful not to distort facts to fit them into the analogy no matter how striking.

According to an article in the *Saturday Evening Post*, Feb. 18, 1950, computers are subject to psychopathic states which the engineer in charge cures by a "shock treatment" consisting of the application of excessively large voltages. I would be interested to know whether this is a "might be" or an "is." So far, I have been unable to find anyone who recommends quite so slap-dash a method of trouble-shooting. It would be too much like dropping a valuable watch on the floor to improve its time-keeping ability; granted that this treatment would work once in a while, it hardly seems the economical procedure in the long run.

Another "might be" is the checking method that the reader of the public press would infer is generally used, with three parallel computing elements, all doing the same problem and voting on the correct answer. A majority vote decides the answer that the computer will print. There may be such a machine, despite the low economy of this checking method, but to date I have been unable to find this remarkably democratic device.

The listing of "might be's" could be extended to greater length. I should like to think, however, that I have touched upon a matter of concern to the entire scientific fraternity and that it is unnecessary to belabor my point. In all sincerity, I am urging more care and restraint in reporting scientific work to the public, particularly when the person reporting has only a secondary interest in that work and is likely to be misled by incomplete information.

G. R. STIBITZ

Burlington, Vermont

BIBLIOGRAPHY Z–XII

1. E. G. ANDREWS & H. W. BODE, "Use of relay digital computer," *Electrical Engineering*, v. 69, 1950, p. 158–163.

Use of two Bell Laboratories large-scale digital computers is described; discussion of process of setting up problem, decisions which must be made by attending mathematician, and those decisions which can be left to machines are noted; samples of different types of problems which have been solved successfully by machines are given; and procedures used are discussed.

EDITH T. NORRIS

NBSMDL

2. ANON., *Description and Use of the ENIAC Converter Code*, Ballistic Research Laboratories, *Technical Note* No. 141, Aberdeen Proving Ground, Maryland, November 1949, 23 pages. Mimeographed.

In the first three years of its existence, the ENIAC, in spite of its frequent and often prolonged breakdowns, executed its tasks so speedily that the attending crew of programmers found it exceedingly hard to keep pace with its operation. The introduction of a set of coded orders by JOHN VON NEUMANN and Aberdeen's mathematical staff materially lessened the effort and time consumed by the attendants in supplying problems for the ENIAC. A new unit, the Converter, was incorporated which receives the code digits and initiates the corresponding operations. The machine operates on a one-address control system.

The list of orders falls into essentially three categories. The storage orders call for the machine to perform the following operations:

a) Transmit information from an IBM card to the eight Transmitter Groups, each holding a signed 10-decimal-digit number.
b) Transmit information from the above eight groups and from an additional pair of similar nature to 20 Registers (18 of which are misnamed Accumulators, as pointed out by the authors themselves), each holding a signed 10-decimal-digit number.
c) Transmit information from the three Function Tables to the above Registers. (A Function Table consists of 104 lines, each holding two signed six-digit numbers or a sequence of coded instructions. Each line bears a three-digit address.)

The arithmetic orders call for the machine to perform the following operations:

a) Add a number to the contents of an Accumulator.
b) Subtract a number from zero.
c) Multiply two numbers with single precision, and add the product to a third number.
d) Divide two numbers with single precision, with remainder available.
e) Extract square root, with remainder available.
f) Obtain the absolute value of a number.
g) Obtain $(1 - N)10^k$, where N is a number whose decimal point is k places from the left.
h) Multiply a number by 10^p, where $-5 \leq p \leq 5$. (These shift orders are of two types, allowing for the retention of the shifted-out digits in another Register, or for their deletion.)

The control orders call for the machine to perform the following operations:

a) Transfer Control—both conditionally and unconditionally.
b) Count in order to facilitate iterations.
c) Delay and stop.

The publication gives a careful explanation of each order but unfortunately exhibits some of the ills always accompanying the appending of an "afterthought." For instance, the letters A and B are used to indicate the first two Transmitter Groups, as well as the two sides of each Function Table line. The letter X, often misprinted as x, represents the Multiplication Code as well as an arbitrary number within a register. A slightly more serious error is the wrong illustration of order 6L, at the top of page 10, which accompanies the correct verbal explanation.

The interested reader would like to know whether there is any provision in the ENIAC for detecting overflow on addition and whether the multiplication order gives a rounded product. This technical note was designed for use within the Ballistic Research Laboratories and was written primarily for issuing available information when the occasion demands speed. The exposition of the codes is valuable in that it is sufficiently clear to enable any reader to attempt programming computations on the ENIAC.

IDA RHODES

NBSMDL

3. ANON., *Digital Computer Research at Birkbeck College*, Office of Naval Research (London Branch), *Technical Report* OANAR-50-49, 12 December 1949, 2 p.

This report describes the design features and operating characteristics of the three digital computers being constructed under the direction of A. D. BOOTH of Birkbeck College, University of London. They are the automatic relay computer (ARC), the simple electronic computer (SEC), and the all-purpose electronic x-ray computer (APEXC).

The ARC is a part relay, part electronic parallel machine using magnetic drum storage. Teletype tape is used as an input medium, and data is entered into the machine in binary form. A teleprinter or tape perforator will be used for output. Several simple problems have been run on this machine such as tabulation of prime numbers and factorization of large numbers. Although it is now temporarily dismantled, it will be reassembled and will use cross-bar type memory units.

The SEC is a small, all-electronic, parallel calculator. It has the same type of magnetic drum memory as the ARC; teletype is used for input and output.

The APEXC will be an evolution of the SEC using a magnetic drum store and employing about 800 vacuum tubes. The machine will store 1,024 numbers of 32 binary digits. Input and output will be on magnetic tape. The machine will be used initially for making crystallographic computations.

EDITH T. NORRIS

NBSMDL

4. ANON., *The EDSAC Computing Machine, Cambridge University*, Office of Naval Research (London Branch), *Technical Report* OANAR-43-49, 25 November 1949, 5 p.

This report describes the design features and present use of the EDSAC built by M. V. WILKES and his co-workers at the University Mathematical Laboratory, Cambridge, England. [See *MTAC*, v. 4, p. 61–65.] In

order to gain experience with the programming of problems on the EDSAC, a number of simple computational problems have been run on the machine (e.g., the calculation of prime numbers, tabulation of the complex gamma function [UMT 102], computation of the number "e" to 200 decimal places, and calculation of the AIRY integrals).

EDITH T. NORRIS

NBSMDL

5. WARREN S. MCCULLOCH & JOHN PFEIFFER, "Of digital computers called brains," *The Scientific Monthly*, v. 69, 1949, p. 368–376.

Comparison between known operations in the human brain and similar operations in large-scale computers.

6. H. J. MCSKIMIN, "Theoretical analysis of the mercury delay line," Acoustical Society of America, *Jn.*, v. 20, 1948, p. 418–424, 4 figs., 2 tables.

The electromechanical aspects of problems presented by the use of mercury delay lines in computers are discussed. After a brief discourse on the theory of wave propagation for liquids, an analysis is made of the voltage developed by the piezoelectric pick-up crystal used in the delay line and of the distortion that might result when the carrier pulse is modulated. It is found that waves with slightly differing phase velocities can exist and may produce distortion effects.

EDITH T. NORRIS

NBSMDL

7. R. D. RICHTMYER & N. C. METROPOLIS, "Modern computing," *Physics Today*, v. 2, Oct. 1949, p. 8–15.

Developments during the last decade of automatic computing methods with rapid progress involving engineering principles and techniques, mathematical methods, and logic of automatic computation are discussed. Also described are the functions of the ENIAC, methods of presenting problems to computing machines, possibilities of using machines for analytic purposes, and practical uses of computers in their present stage of development.

EDITH T. NORRIS

NBSMDL

8. A. E. SMITH & C. V. L. SMITH, "Digital computers and their applications," American Society of Naval Engineers, *Jn.*, v. 61, 1949, p. 137–168, diags.

Presented herein is a general discussion of the design principles of digital computers and a description of existing machines and those under development.

NEWS

Association for Computing Machinery.—Rutgers University was host to members of the Association at a conference on automatic computing machinery. The conference included general sessions on Tuesday morning and evening, March 28, plus two parallel groups of sectional meetings designated as Section A and Section B, March 28 and 29.

In Section A, the talks dealt with applications of computers, engineering descriptions of several complete machines, and engineering problems encountered in the design of machine components. Section B was concerned with the mathematical aspects of the design of automatic computers, the coding of complete problems to be solved on the machines, and mathematical descriptions of complete machines.

In addition to the program of talks, the following exhibits were shown: the REAC by the Reeves Instrument Corporation, the RCA Linear Simultaneous Equation Solver by the RCA Laboratories, the IBM Card-Programmed Electronic Calculator by the International Business Machines Corporation, the small Binary-Octal Calculator by the Raytheon Manufacturing Company, the MADDIDA (Magnetic Drum Digital Differential Analyzer) by Northrop Aircraft, Incorporated, the oscillograph in the computer field by Allen B. DuMont Company, and Zator card equipment by the Zator Company.

The program was as follows:

General Session, Tuesday, March 28, Dean ELMER C. EASTON, College of Engineering, Rutgers Univ., presiding:

Welcoming address by MASON W. GROSS, Provost, Rutgers University.

"High speed computing machines—a survey," PERRY CRAWFORD, Research and Development Board.

"Machines of moderate cost," GEORGE STIBITZ, Burlington, Vt.

Section A, EDWARD W. CANNON, National Bureau of Standards, presiding.

"Applications of computing machines to the solution of management problems," MARSHALL K. WOOD, Department of the Air Force.

"Engineering applications of electronic analog computers," HERBERT ZAGOR, Reeves Instrument Corporation.

"Applications of electronic computers to Census Bureau problems," JAMES L. MCPHERSON, FLORENCE K. KOONS, RALPH E. MULLENDORE, Bureau of Census.

"Applications of the BINAC," JOHN W. MAUCHLY, Eckert-Mauchly Computer Corporation.

Section B, FRED G. FENDER, Rutgers University, presiding.

"The BINAC—a technical report," JAMES R. WEINER, Eckert-Mauchly Computer Corporation.

"An analog series computer," MAX G. SCHERBERG, Office of Air Research.

"Preliminary design of the Mark IV," BENJAMIN L. MOORE, Harvard Univ.

"Design of a low-cost computer" (read by C. V. L. SMITH), PAUL L. MORTON, Univ. of Calif.

General Session, banquet, HOUSTON PETERSON, Rutgers Univ., toastmaster.

"Automatic computing machinery of moderate cost," HOWARD H. AIKEN, Director, Computation Laboratory, Harvard Univ.

Section A, Wednesday, March 29, JAMES J. SLADE, Jr., Rutgers Univ., presiding.

"A digital computer for solution of simultaneous linear equations," SAMUEL LUBKIN, Electronic Computer Corporation.

"The ANACON, a large-scale general-purpose analog computer," D. L. WHITEHEAD, Westinghouse Electric Corporation.

"The IBM card-programmed electronic calculator," CUTHBERT C. HURD, International Business Machines Corporation.

"The MADDIDA, general features," FLOYD G. STEELE, Northrop Aircraft, Inc.

Section B, FRANZ L. ALT, National Bureau of Standards, presiding.

"Planning and error consideration in the numerical integration of a difference equation," FRANCIS J. MURRAY, Columbia Univ.

"Probability methods in the solution of elliptic partial differential equations," JOHN H. CURTISS, National Bureau of Standards.

"A machine method for solution of systems of ordinary differential equations," RICHARD F. CLIPPINGER & BERNARD DIMSDALE, Aberdeen Proving Ground.

"The theory of digital handling of nonnumerical information and its implications to machine economics," CALVIN M. MOOERS, Zator Company.

Section A, ERNEST G. ANDREWS, Bell Telephone Laboratories, presiding.

"New circuits installed in the Aiken relay calculator," FREDERICK G. MILLER, U. S. Naval Proving Ground.

"Digital computing machine components of universal application," WILLIAM S. ELLIOTT, Research Laboratories of Elliott Brothers, Ltd. (London).

"Design features of a magnetic drum information storage system," JOHN L. HILL, Engineering Research Associates, Inc.

"The SB-256 electrostatic selective storage tube," JAN A. RAJCHMAN, RCA Laboratories.

Section B, ELLIS R. OTT, Rutgers Univ., presiding

"Optical ray tracing," DONALD P. FEDER & BENJAMIN HANDY, National Bureau of Standards.

"Solution of matrix equations of high order by an automatic computer," HERBERT F. MITCHELL, Jr., Eckert-Mauchly Computer Corporation.

"Theodolite reductions on the IBM relay calculators," MARK LOTKIN & C. E. JOHNSON, Aberdeen Proving Ground.

"The MADDIDA, design features," DONALD E. ECKDAHL, Northrop Aircraft, Inc.

The Institute of Radio Engineers.—At the 1950 National Convention held in New York City from March 6 through March 8, two sessions were devoted to high-speed computers.

The first session on Wednesday morning, March 8, under the chairmanship of GEORGE R. STIBITZ, dealt exclusively with digital computers. In a paper entitled, "Static magnetic pulse control and information storage," AN WANG of Harvard University mentioned the possibility of developing a digital memory system using magnetic materials having rectangular hysteresis loops to control transfer of electrical pulses through the core by means of the property of residual magnetism. The incorporation of unidirectional current devices permits a static, high-efficiency pulse power distribution system. RALPH SLUTZ of the National Bureau of Standards next discussed the development of a generalized procedure of designing diode circuits for pulse gating, with particular attention to the extremely high reliability required for electronic digital computers. In the third paper, "Marginal checking as an aid to computer reliability," NORMAN H. TAYLOR of M.I.T. pointed out the source of error in digital computing and pulse communication caused by deterioration of machine components. Marginal checking varies voltages in logical circuit groups, inducing inferior parts to cause failure, while a test program or pulse transmission detects and localizes potential failure. By automatically carrying out this marginal checking, a digital computer can act as its own detector. "The development of the California Digital Computer" by DAVID R. BROWN and PAUL L. MORTON, University of California, Berkeley, presented a description of a low-cost general-purpose electronic digital computer having a compact magnetic-drum memory with a capacity for 10,000 ten-decimal-digit numbers. This large memory capacity permits much computation without the necessity of automatic access to input. The average access time is eight milliseconds. Machine input is accomplished on punched paper tape read photoelectrically. Binary-coded decimal numbers pass serially through the arithmetic unit on four parallel channels, and single-address operations (including division and square rooting) will be performed at the rate of about 60 per second. In the final talk of this session JOSEF KATZ, University of Toronto, mentioned a new class of switching tubes designed to reduce the complexity of electronic switching circuitry. The tube electrodes (one for each input and output channel) are designed so that particular combinations of input voltages result in current flow to the corresponding combination of output electrodes. The total current, and hence the cross section of the electron beam, is restricted by a limiting resistor used to focus the beam.

The second computer session on Wednesday afternoon, March 8, under the chairmanship of WILLIAM H. HUGGINS, was concerned with information analysis and computing. The REAC (Reeves Electronic Analog Computer) was described by H. I. ZAGOR, Reeves

Instrument Corporation, New York, as a flexible and practical tool for solving ordinary linear and nonlinear differential equations. In addition, the speaker illustrated the capabilities of the machine components and showed the various techniques involved in solving such representative problems as flutter, electron flow, automatic pilot design, Fourier analysis, engine control, integral and boundary value equations. "An electronic storage system" by E. W. BIVANS and J. V. HARRINGTON, Air Force Research Laboratories, Cambridge, Mass., described the RCA Radechon (a barrier grid storage tube) which is being used in a digital storage system. The secondary collector system is not used; instead, the reading signals are measured at the back plate, the same electrode on which the write signals are impressed. Deflection voltages are generated by a weighted addition of the plate voltages of a binary counter. Read and write operations are asynchronous with a 12-μ sec minimum time between operations. An application of the theory of correlation functions used in the determination of the transfer functions of linear and nonlinear systems was presented next by J. B. WIESNER and Y. W. LEE, M.I.T. In the paper, "Measurement and analysis of noise in a fire-control radar" by R. H. EISENGREIN, Sunstrand Machine Tool Company, Rockford, Illinois, an "instantaneous subtraction" method of optically measuring radar noise in order to analyze the unwanted portion of the signal return from an airborne target was discussed. Finally, H. E. SINGLETON, M.I.T., described a new electronic correlator which is capable of accepting inputs covering a wide frequency range and which evaluates correlation functions for arguments from 0 to 0.1 seconds. In order to obtain a high degree of accuracy and stability, the signals are sampled and converted to binary numbers, and the storage and computation are carried out digitally.

OTHER AIDS TO COMPUTATION

BIBLIOGRAPHY Z–XII

9. D. P. ADAMS & H. T. EVANS, "Developments in the useful circular nomogram," *Rev. Sci. Instruments*, v. 20, 1949, p. 150–154.

A circular nomogram for $W = UV$ with the U, V scales on the circumference and the W scale on a diameter is described, with a discussion of the most advantageous choice of scales.

10. J. A. BRONZO & H. G. COHEN, "Note on analog computer design," *Rev. Sci. Instruments*, v. 20, 1949, p. 101–103.

This note proposes that partial differential equation problems be attacked by transforming them into difference-differential systems and then into systems of linear equations. The characteristic roots of the matrices of the latter are to be investigated by a change of coordinate system. The choice of the new coordinate system is not specified but is dependent on the ingenuity of the investigator.

F. J. M.

11. J. H. FELKER, "Calculator and chart for feedback problems," I.R.E. *Proc.*, v. 37, 1949, p. 1204–1206.

The chart consists essentially of constant-magnitude and constant-phase loci of z in the complex plane of $\gamma = z/(1 + z)$. A calculator based on this chart is available commercially.

LOTFI A. ZADEH

Department of Electrical Engineering
Columbia University