

CALIFORNIA DIGITAL COMPUTER

Sept. 1950

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127. Correction to the article "Matrix Inversion by a Monte-Carlo Process"---in the proof of Theorem 1 of the above article [WTKC, v. 4, p. 127-128] it was tacitly assumed that the sum given for  $E(G)$  was absolutely convergent, since otherwise the first absolute moment of  $G$  and therefore  $E(G)$  fail to exist. We must therefore replace assumption (1) of the article by a stronger hypothesis, namely

## The California Digital Computer

The California Digital Computer (CALDIC) is to be operated by the Engineering Department of the University of California at Berkeley for the benefit of its own research and that of the other departments and for the instruction of graduate students. This fact has strongly affected its logical design (in the hope of avoiding a large highly-trained staff) and also its physical design (requiring all parts to be accessible for demonstration and servicing). It is strictly a low-cost machine and makes no claims to superiority in speed or originality in design; most of the electronic techniques used are well established. It is not, however, designed for maximum simplicity of construction but rather for simplicity of description to and operation by the varied group of scientists who are expected to bring their computing to it. Its operation is to be straight-forward and as nearly like the familiar hand computational methods as possible, at least until experience is gained in its use. Its construction permits easy modification in the future, and it is expected that such modification will occur.

The frontispiece shows most of the portions of the computer which are completed at this writing (September 1, 1950). At the left is the memory unit, consisting of a vertical rotating drum with four columns of combination reading-recording heads arranged around it and a set of electronic panels approximately six feet high by ten feet wide which contain the circuitry required to write into and read from the drum. To the right of these is the first of the arithmetic registers; the second has been built but not yet installed on the blank panels below. At the extreme right is the order counter which is a shifting and counting register designed to store and supply the address of the next order to be carried out. The panels shown, a few of which are temporary, were built first to allow their operation as a test system, and, as other parts of the computer are completed, they will be added to the system.

Figure 1 shows a simplified block diagram of the computer. It is a serial machine so far as decimal numbers are concerned; but the binary parts of each digit are transmitted in parallel, and most of the circuits have four channels. The three arithmetic registers are of the shifting type, with circulation paths provided as shown. The "A" or accumulator register incorporates an adder in its first column, and circulation of its contents simultaneously with receipt of a new number causes the sum to appear and stand in the register. For multiplication the "D" register holds the multiplicand, which is repeatedly circulated but simultaneously shifted and added into the A register as required by the digits of the multiplier which are drawn from the "R" register. As the multiplier digits are used the overflow from the A register appears in their places, and at the end of the process the double-length product occupies both the A and the R registers.

All timing pulses for the computer are drawn from a timing track permanently recorded on the drum, and therefore no effort to control the drum speed is needed. A small gap in the timing track is used to provide an "origin pulse," and recorded words are located by counting the timing pulses, beginning the count at the origin. Information recorded on the drum is therefore not lost during power failures or other shut-downs; subroutines could

be permanently stored if desired. The timing pulses are divided by suitable circuits into "digit pulses" in groups of eleven which provide for shifting numbers through the registers and "space pulses" which occur between the groups of digit pulses and which initiate all switching.

### COMPUTER BLOCK DIAGRAM

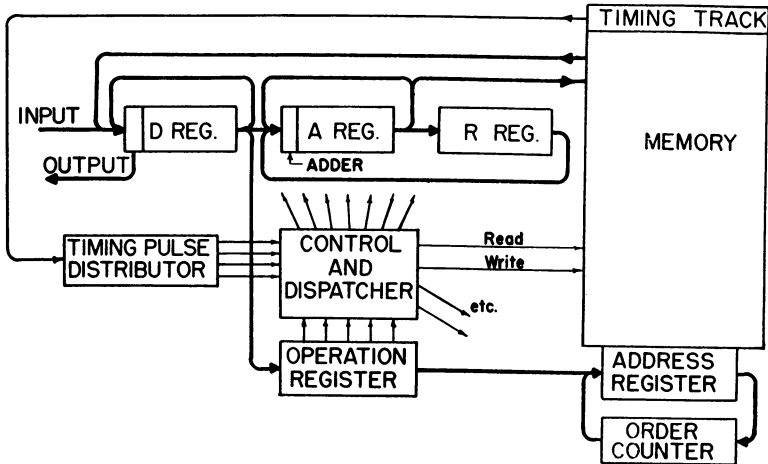


FIGURE 1

The operation of the computer will be cyclic, essentially as follows:

1. The address of the next order to be performed is shifted from the order counter to the address register and used to extract the order from the memory into the D register.

2. The order is shifted into the operation and address registers, and simultaneously the contents of the address register are returned to the order counter and increased by one to provide for the next cycle.

3. The address register now contains the address of the operand, which is withdrawn from the memory into the D register and operated on as required by the contents of the operation register. At the end of the cycle the result stands in the A register.

The normal cycle requires two trips to the memory, each of which might take almost the time of a full drum revolution (17 milliseconds) in addition to the time required for the operation itself which is usually small in comparison. In most cases, however, the orders will be in consecutive memory boxes and the whole cycle will require only slightly more than the time of one revolution. In addition, the consecutively-numbered boxes are spaced around the drum at intervals which correspond to the time required for an addition and order-shift, and recognition of this fact in programming may make it possible to carry out as many as ten operations per revolution of the drum. Abnormal cycles are used for several orders for which no new operand is needed; shift-left, shift-right, and sub-program orders are of this type. The cycle time for these, however, is about the same as for normal cycles. Multiplication and division, which are performed by repeated addition, may

require an additional revolution. Because of these variations the average operation speed is difficult to estimate, but it should be considerably better than 50 single-address operations per second on most problems.

The orders to be provided are: add, subtract, multiply, multiply and round off, divide, divide and round off, extract the square root, read the input tape, transfer to memory, print out, clear address and add, change contents of order counter, change contents of order counter but only if the previous operation overflowed, shift left, and shift right.

The only unusual orders are the "clear and add" and the conditional sub-program orders. The former provides for the modification of orders by building the desired address in the A register and attaching the operation part of the order to it. The latter provides for discrimination and also for overflow of the accumulator; a possible overflow is provided for by inserting

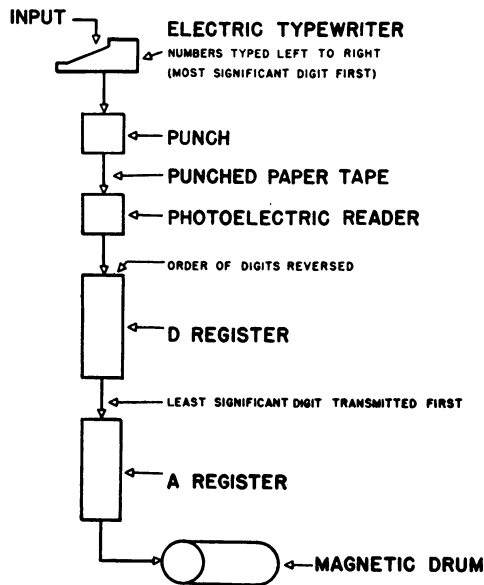


FIGURE 2

the instruction which tells the computer what to do if the overflow occurs. If no overflow occurs, the instruction is disregarded.

Orders consist of two decimal digits which specify the operation and four additional digits which usually specify the location in the memory of the operand, but sometimes they give other information such as the location of a sub-routine or the number of places of shifting in a shift-left order. No use is made of the sign column or the remaining four digit positions of the normal 10-decimal-digit word.

Input will be from perforated tape, using the system diagrammed in Figure 2. In general all orders and data will be stored in the memory at the beginning of a problem, and the input will not be consulted further during the computation. The "read the input" order is designed mainly to instruct the machine to proceed to the next problem when one is completed; the tape reader will be loaded manually, and the tape will be run clear through on

receipt of the "read" order. The information read from the tape may, however, be placed in any desired portions of the memory, as specified by addresses punched into the tape ahead of the blocks of information. The entire memory can be filled in approximately three minutes. Output also will be through punched tape followed by printing with a standard tape-reading typewriter. Output speed is limited to punch speed of about ten digits per second.

The outstanding feature of the computer is its magnetic memory, shown in more detail in Figure 3. The drum is about eight inches in diameter and

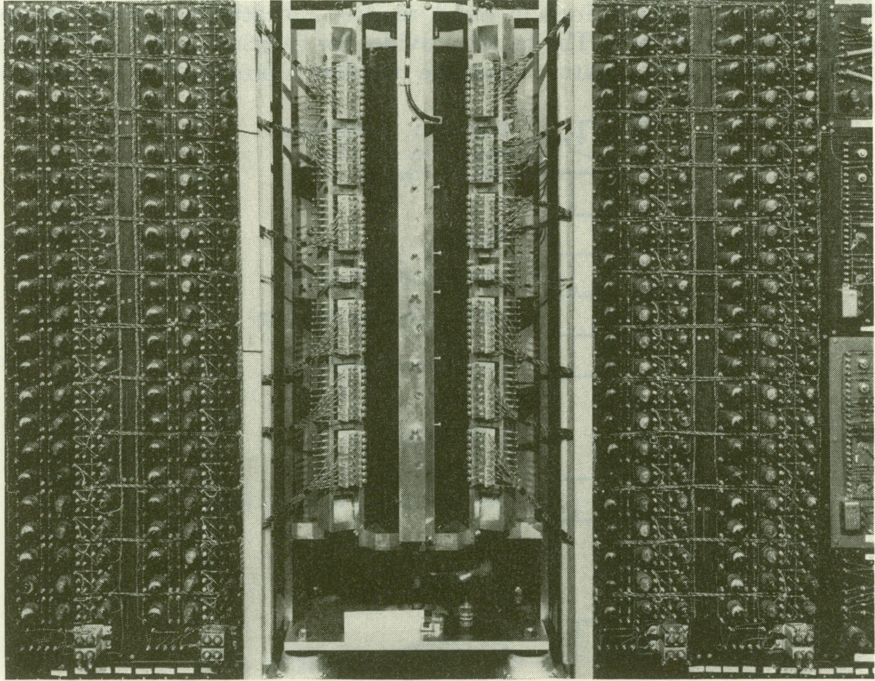


FIGURE 3. Magnetic Memory

26 inches long and will store 10,000 ten-digit numbers with their signs. Since the no-excess binary code is used, over 480,000 memory cells are required at a density of about 900 per square inch of surface. There are 200 specially-designed magnetic reading-recording heads, and each is provided with a writing tube, a writing gate, and a reading gate. In addition 50 tubes are used in the band switch, and with the timing circuits and the 4-channel reading and writing amplifier circuits the memory unit requires about 750 tube envelopes, many of them double triodes. This is more than half of the approximately 1300 tubes used in the whole computer along with 1000 crystal diodes.

Practically all of the design and construction of the CALDIC is the work of graduate and undergraduate students in Electrical Engineering, some 35 having been associated with the project already. The electronic work is now being supplemented by research and instruction on programming and applications. The need for both types of training is demonstrated by the demand

which has developed for graduates of the program. Financial support from the Mathematics Branch of the Office of Naval Research has made the work possible, and techniques developed by other ONR-supported projects have been used freely.

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## Step-by-Step Integration of $\ddot{x} = f(x, y, z, t)$ without a "Corrector"

**Introduction.**—For step-by-step numerical integration of ordinary differential equations there are too many formulae, too few evaluations or comparisons. Perhaps the complexity of the subject will not permit the generalizations the mathematician would prefer, but only restricted numerical comparisons of specific procedures. This paper, at any rate, will restrict itself to showing reasons for preferring one of two procedures for the integration of second-order differential equations in which the second derivative,  $\ddot{x} = \frac{d^2x}{dt^2}$ , is a function of  $x$  alone, or of  $x$  and  $t$ , or of  $x, y, z, t$  (with similar equations for  $\ddot{y}$  and  $\ddot{z}$ ). These equations are important, of course, in certain dynamical problems of astronomy, ballistics, aerodynamics, etc., including the rocket problem.

The comparison of the two procedures will extend to at least three equivalent forms, in which the integration formula at each step is based upon

- (a) antecedent values of  $\ddot{x}$ ,
- (b) backwards differences of  $\ddot{x}$ ,
- (c) central differences (estimated) of  $\ddot{x}$ .

Although there are reasons for preferring forms (a) or (b) in certain circumstances, the comparison will be made first between the procedures in form (c) because there is some advantage to distinguishing between errors of estimation and errors resulting from the neglect of higher order terms in the integration formulae.

The preferred procedure, designated the "second-sum procedure" or " $\Sigma^2$  procedure," involves tables of  $\ddot{x}$  and its first and second sums,  $\Sigma\ddot{x}$  and  $\Sigma^2\ddot{x}$ , as well as its differences (explicitly or implicitly),  $\delta\ddot{x}$ ,  $\delta^2\ddot{x}$ ,  $\delta^3\ddot{x}$ ,  $\dots$ . It has been used for more than a century by astronomers,<sup>1,2</sup> but has apparently been overlooked by a number of mathematicians, physicists, and others, in recent years.

The compared procedure, designated the "second-difference procedure" or " $\delta^2$  procedure," involves the summation (explicit or implicit) of the second difference of  $x$ ,  $\delta^2x$ , which is obtained by formula from  $\ddot{x}$  and its differences (or the equivalent). This procedure was used by COWELL & CROMMELIN, perhaps for the first time in an extended calculation, in their celebrated prediction of the return of Halley's Comet in 1910. In publishing the results of this work<sup>3</sup> they recommended without explanation, however, that future integrations of this type should be done with the  $\Sigma^2$  procedure and formulae. In spite of this recommendation a great deal of work has been done by the