UNPUBLISHED MATHEMATICAL TABLES

156[A].—M. K. PAGE & M. K. PFEIL, *Further Computation of the Digits of e.* One page tabulated from punched cards. Deposited in the UMT FILE.

This gives the value of e to 3333D as obtained on the IBM 604 calculating punch. This work supplements that of F. GRUENBERGER and O. MARLOWE as reported in *MTAC*, v. 6, p. 123–124. The remainders of the various terms at 3333D and 3347D will be furnished upon request.

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M. K. PFEIL

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157[A].—J. W. WRENCH, JR., Log π *and Related Values.* One typewritten page deposited in the UMT FILE.

The values of $\ln \pi$, $\log \pi$, $\frac{1}{2} \ln 2\pi$, $\frac{1}{2} \log 2\pi$, and $\log 2$ are given to 329D. The first of these was computed from

$$\ln \pi = \ln (2^{10} \cdot 3 \cdot 7^6 \cdot 17^5) - 4 \log (5^2 \cdot 11 \cdot 13) + \log (1 - \epsilon)$$

where ϵ is approximately $2.51869 \cdot 10^{-9}$. These values confirm the 214D values published by UHLER.[1]

J. W. WRENCH, JR.

4711 Davenport St., N.W.
Washington 16, D. C.

[1] H. S. UHLER, "Log π and other basic constants," Nat. Acad. Sci., Washington, *Proc.*, v. 24, 1938, p. 23–30.

158[F].—A. GLODEN, *Solutions of* $x^4 + 1 \equiv 0 \pmod{p}$ *for* $600000 < p < 800000$. Typewritten manuscript, 22 p. Deposited in the UMT FILE.

This is a continuation of two previous tables for $p < 600000$ [*MTAC*, v. 3, p. 96]. The present table gives two solutions for every possible prime p between 600000 and 800000.

With the help of these tables various results on the factors of $x^4 + 1$ were obtained, such as

$$820^4 + 1 = 626929 \cdot 721169.$$

These are appended.

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AUTOMATIC COMPUTING MACHINERY

Edited by the Staff of the Machine Development Laboratory of the National Bureau of Standards. Correspondence regarding the Section should be directed to Dr. E. W. CANNON, 415 South Building, National Bureau of Standards, Washington 25, D. C.

TECHNICAL DEVELOPMENTS

THE ELECTRONIC COMPUTER AT THE INSTITUTE FOR ADVANCED STUDY

An all-electronic, general purpose, digital computer has been in operation at the Institute for Advanced Study in Princeton, New Jersey, since June 1952.

The overall characteristics of the Institute machine are displayed below and may be seen to follow closely the requirements established by BURKS, GOLDSTINE and VON NEUMANN in June 1946.

MACHINE CHARACTERISTICS

OVERALL

Binary
Parallel
40 bit words
2300 thermionic tubes
$2' \times 6' \times 8'$ in size
16 kilowatts of power

CONTROL

1-Address code with each 40 digit word containing two 20 digit orders
Asynchronous
Direct coupled
20 basic instructions
10 bit instructions

MEMORY

William's type electrostatic storage
1024 word capacity
40 parallel stages
Standard 5CP1A cathode ray tubes
Synchronous memory control
24 μs. period

ARITHMETIC

Completely direct coupled
Fixed binary point
Complemented representation of negative numbers
All numbers $-1 \leq x < +1$
12 μs. carry time
60 μs. addition order time
700 μs. average multiplication order time
1100 μs. division order time

INPUT–OUTPUT

IBM PUNCHED CARD

12 words per card
40 binary digits per word
100 cards per minute—load
100 cards per minute—punch

TELETYPE TAPE

5 holes across
4 bits information
8 minutes per 1024 words—load
32 minutes per 1024 words—print
16 minutes per 1024 words—punch

MAGNETIC DRUM

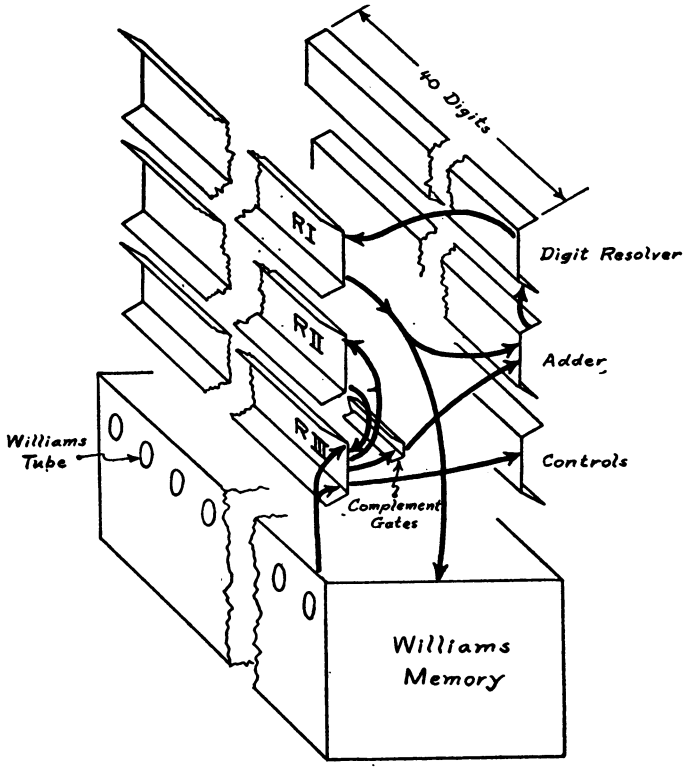
In process

The translation of the preliminary principles of logical design into a working high-speed machine was accomplished by a small group of engineers and technicians directed by JULIAN H. BIGELOW. Bigelow's design disciplines were:

(a) Compactness, achieved by seeking optimum geometrical distribution of components, to minimize the effect of the purely parisitic interconnections.
(b) Minimization of the number of tubes, achieved by (a) along with the elimination of logical redundancies and special purpose circuitry.
(c) Logical operations independent of signal waveforms.

(d) Sequential control operation with each key operation initiated by the safe completion of the preceding operation.
(e) Safe circuit operation between essentially zero duty cycle and its maximum safe repetition rate since the duty cycle over a long period of varied computations could not be predicted.
(f) All of the above bounded by very conservative design criteria for the components.

The major departure of the final machine from the proposals of the 1946 report is the use of the Williams storage phenomena in a cathode ray tube memory. The 40-stage memory with a capacity of 1024 words was developed by JAMES H. POMERENE and Bigelow.



SCHEMATIC OF BASIC CONNECTIONS BETWEEN WILLIAMS MEMORY, CONTROL, AND ARITHMETIC UNITS

FIG. 1.

Structure.

The frontispiece shows a view of the Institute machine.

Figure 1 is a schematic establishing the physical layout of the machine and displaying the interconnections between the Memory, Control, and Arithmetic Units.

The large block at the bottom contains the 40 cathode ray tubes (5CP1A), 20 on each side. Each memory tube has an associated three stage amplifier and an eight tube discriminator unit which controls the beam turn-on.

The upper portion contains the arithmetic and control organs. On the left there are three double rank registers each containing two rows of 40 flip-flops and two rows of gate tubes for entry into them. The left-most stage contains the most significant digit. The machine is designed to accommodate numbers in the range $-1 \leq x < +1$, with negative numbers handled in the complemented representation. The most significant digit thus becomes the sign indicator with the binary point fixed to the right of it.

The register labelled RI is called the Accumulator. It is a double rank shifting register which holds the resident number and then the final sum during an addition, the partial remainders during division and the most significant digits of the partial products during multiplication.

RII is called the Arithmetic Register. It is a double rank shifting register which holds the multiplier and the least significant digits of the partial products during multiplication and the quotient during division.

RIII is a non-shifting Memory Register. In the upper row of 40 flip-flops it receives *numbers* from the memory and presents them to the adder via the 40 complementing gates. It contains the incident number during addition, the multiplicand during multiplication and the divisor during division. In the lower row of flip-flops it receives *order-pairs* from the memory, each half containing a ten digit address and a ten digit instruction. Since order-pairs and numerical data are indistinguishable outside of the process in which they are used, any order-pair may be altered by bringing it from the memory to the arithmetic organ via the upper row of RIII, performing an arithmetic operation on it and storing the result back in the memory.

On the right the row of adder chassis contains 40 parallel circuits each receiving three inputs; the resident digit from RI, the incident digit from RIII (upper) via the complement gates, and a carry digit from the next less significant stage. The adder circuit contains four tubes which propagate a carry to the next stage and reduce the eight possible inputs to four possible voltage levels. The row of chassis above the adder is called the digit resolver and reduces the four voltage levels coming out of the adder to two voltage levels representing a "1" or a "0". This information is then communicated to RI.

The lower row of chassis comprise the control organ containing four major units: the main control, the shift counter, the address counter, and the memory control.

1) The main control establishes the sequence for observing the two halves of any order pair and bringing up a new order. It decodes the order digits and commands the execution of the resulting process. It is completely asynchronous. It does not go through the expense of matrix decoding, but rather utilizes unique logical combinations of several order digits to command the desired process.

2) The shift counter counts the number of shifts in the shifting registers and contains recognition circuits which determine when shifting shall be terminated appropriately to the order being done.

3) The memory control with its associated pulse chain establishes reading and writing routines under the command of the main control, and, independently, routines to control the regeneration of the static information in the memory.

4) The address counter remembers the locations of the last point regenerated on the face of the cathode ray tube and of the last order-pair executed; advancing these addresses by one each time. It is also capable of receiving from RIII, however, the address associated with any instruction. During every memory cycle one of the above addresses is used to command the deflection of the cathode ray beams.

Memory.

During any period of time in which the memory is not specifically involved in delivering information to or receiving information from the arithmetic organ, the memory control reverts back to sequential regeneration of the 32 × 32 words stored on the phosphor surfaces of the 40 cathode ray tubes. The timing of this process is governed by a clock and associated pulse chain, with a 24 μs. period. Within this period there is one moment when the memory control is receptive to intervention by the main control. The main control may at this time be specifying one of the following processes:

(a) Bring the next order-pair of a consecutive series of orders into the lower row of 40 toggles in the memory register RIII.
(b) Depart from this consecutive series of orders to bring a new order-pair into the lower row of the memory register RIII from an address specified by a "transfer control" order in RIII.
(c) Bring a number into the upper row of the memory register RIII from the address specified by the order in RIII.
(d) Store the number residing in the accumulator register RI at the address specified by the order in RIII.

The memory control reports back to the main control when it accepts the main control intervention and when it completes any of the actions described in (a)–(d). In this manner the synchronous memory operation is safely incorporated into the asynchronous arithmetic process.

The inherent coupling between adjacent storage locations on the face of any cathode ray tube places a limit on the number of times any point on the raster may be consulted before its neighbors are regenerated. For the Institute machine this number, called the "read around" ratio, is in the neighborhood of 30.

Arithmetic and Control Operations.

The twenty basic orders executed by the Institute machine are listed below with the average time per order measured in a long sequence of similar orders. Many of the processes are operating with inordinate factors of safety. Thus the speed figures below reflect the present arbitrary state of adjustment of the machine, not its maximum capabilities.

(1–8) *Add*.....62 μ.s.

Bring a number from position x in the memory and add it to the number residing in the accumulator with the following choices:

(a) "Clear" or "Hold" where "Clear" signifies the desire to preclear the accumulator to zero.

(b) "Magnitude" or "Number" where "Magnitude" signifies that the absolute magnitude of the quantity at x is to be added.

(c) "−" or "+".

(9) *Multiply:* Multiplier all ones.....990 μ.s.
Multiplier all zeros.....435 μ.s.
Multiplier half ones.....720 μ.s.

Bring a number from position x in the memory and multiply it by the number residing in the Arithmetic Shifting Register, RII. This order has choice of "Round off."

(10) *Divide*.....1100 μ.s.

Divide the number in the Accumulator by a number to be brought up from position x in the memory.

(11) *Load RII*.....65 μ.s.

Bring a number from position x in the memory and place that number in the Arithmetic Shifting Register, RII.

(12) *Left Shift*.....42 μ.s. + 8 μ.s./shift

Shift the numbers in the Accumulator register, RI and the Arithmetic Shifting Register RII, $n(\leq 47)$ places to the left. During this process the contents of RI shift end around into the right end of RII. However, only zeros are propagated through the right end of RI. The number n is stated in the address portion of the order.

(13) *Right Shift*.....42 μ.s. + 8 μ.s./shift

Shift the numbers in the Accumulator register RI and the Arithmetic Shifting Register RII $n(\leq 47)$ places to the right. During this process the contents of RI shift end around into the left end of RII. However, only the sign digit of the original quantity in RI is propagated through the left end of RI. The right shift order has the choice of Round Off. If Round Off is chosen, 2^{-39} is added into the quantity in RI at the end of "n" right shifts and a total of $n + 1$ shifts are executed.

(14) *Store*.....58 μ.s.

Take the number existing in the Accumulator register RI and store it at position x in the memory.

(15) *Parity Unconditional Transfer*.....39 μ.s.

Bring a new order pair into the lower rank of the Memory Register, RIII from position x in the memory and proceed to observe that order which occupies the same half of the order pair as the unconditional transfer being executed.

(16) *Non-Parity Unconditional Transfer*.....39 μ.s.

Bring a new order pair into the lower rank of the Memory Register, RIII from position x in the memory and proceed to observe that order which occupies the half of the order pair *opposite* to that occupied by the unconditional transfer being executed.

(17–18) *Parity and Non-Parity Conditional Transfers*.....39 μ.s.

If the number in the accumulator is positive, execute operations described in 15 and 16.

If the number in the accumulator is negative, ignore the request for transfer and proceed to the next order in sequence.

(19) *RII...> RI*.....50 μ.s.

Take the number in the Arithmetic Shifting Register RII and add it to the quantity in the accumulator register RI. This order includes all of the eight variants described in orders (1–8).

(20) *Input-Output Order*

(a) IBM

(1) Input.....n/100 min.
Transfer 12 n words from n IBM punched cards to the 12 n memory addresses starting at address x.

(2) Output.....n/100 min.
Transfer 12 n words from the memory addresses starting at address x to n IBM cards.

(b) Magnetic Drum

(a) Input.....Approx $(150 + 3n)$ milliseconds.
Transfer 32 n words starting with block n_0 of Track A or B from the magnetic drum to the 32 n memory addresses starting at address x $(1 \leq n \leq 32;\ 0 \leq n_0 \leq 31)$.

(2) Output.....Approx $(150 + 3n)$ milliseconds.
Transfer 32 n words from the memory addresses starting at address x to the n Blocks of track A or B of the magnetic drum following the starting Block n_0.

Operating Experiences.

During the first year of machine operation, a considerable amount of time was spent in strengthening weak points in the machine. Towards the latter part of the year the machine came under control with a routine maintenance program permitting long periods of uninterrupted computation.

The bulk of the machine's useful computation time has been devoted to the solution of sets of partial differential equations representing simplified models of the atmosphere. These problems were formulated by a group led by J. G. CHARNEY. In addition, problems in number theory, matrix inversion, and integral equations have been solved by its circuitry. These problems required about 3×10^8 multiplications with the time split fairly evenly between automatic computation and input-output.

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BIBLIOGRAPHY Z

1016. BRUNO DE FINETTI, *Macchine "che pensano" (e che fanno pensare)*, Pubblicazioni delle Facolta di Scienze e di Ingegneria dell'Universita di Trieste, 1952, 34 p., 23.4 × 29.5 cm.

This brochure contains an expository treatment of the automatic digital computer of our era, seen through the eyes of a mathematician and philosopher. Technical details of machine design, being of minor importance to him, are relegated to an appendix which includes photographs and descriptions of some individual machines and the inevitable summary table of speeds and memory capacities. While this appendix is purposely incomplete and not too stimulating, the main part of the booklet is written with a depth of understanding and a clarity and conciseness of expression seldom found in this field. To a reader who knows nothing of computing machines, it explains the relationships between their development and such fields as neurophysiology and psychology, formal logic, information theory, and cybernetics.

It explains the basic functions and components of automatic digital computers, the essential steps involved in programming and coding, the design of "subroutines," and their assembly into comprehensive routines. It touches upon the major classes of computational problems, evaluation of functions and use of tables, matrix inversion and numerical integration of ordinary and partial differential equations. There is a section on relaxation methods and one on the Monte Carlo method. In each of these subjects the fundamental features are adequately brought out in just a few sentences. While it is not clear why the author arranged his topics the way he did, their selection and presentation leaves nothing to be desired.

F. L. ALT

NBSNAML

1017. F. GRUENBERGER, *Computing Manual*, The University of Wisconsin Press, Madison, 1952, 123 p., 15.5 × 23.5 cm. Price $2.00.

This manual was used as a text in a course entitled "Theory and Operation of Computing Machines" held at the University of Wisconsin during 1951 and 1952. The author discusses IBM techniques for chi-squared analysis, random sampling, questionnaires, bivariate tables and differencing. He also presents miscellaneous operating hints for the IBM laboratory worker.

R. K. ANDERSON

NBSCL

1018. H. D. & V. R. HUSKEY, "Electronic computers aiding management control," *The Journal of Accountancy*, Jan. 1952, p. 69–75.

In this very informative article, the authors point out the many economies which may be effected by the use of electronic computation in business administration. Not only would present-day calculations be carried out more efficiently, but the savings in labor, time, and expense would enable various organizations to undertake the solutions of problems hitherto considered prohibitive, for example, the forecasting of trends, as based upon ac-

cumulated data. The recent election prediction carried out by the UNIVAC amply confirms this statement made several months before Election Day by the authors.

The authors indicate some of the factors which account for the economies realized from the use of the electronic computers, such as the immense speed of internal computation. For example, in the time it takes to say the word "multiplication," some computers can perform about 2500 multiplications, or 6000 additions, of pairs of ten-digit numbers. Moreover, these machines are constructed to recognize, and cause automatically the execution of, instructions to perform numerical operations. The resulting elimination of human intervention is a potent time-saver indeed; it also permits a considerable reduction in personnel and in space requirements.

A brief but illuminating history of high-speed computing machines concludes this excellent article.

The reviewer is left with the feeling, however, that the authors give too optimistic a concept of the prowess of the present-day machines as applied to business needs. The prodigious feats of computation which they have exhibited do not apply to all classes of problems. Where defense tasks are concerned, the astounding reduction in time required for their solution is an advantage far outweighing any other considerations. But business managers cannot expect any spectacular savings in dollars and cents until efficient electronic sorter-collators and files allowing random access have been perfected.

IDA RHODES

NBSCL

1019. H. KENOSIAN, "Unitized pulse circuits speed computer design," *Electronics*, v. 25, no. 10, Oct. 1952, p. 156–157.

These unitized pulse circuits were originally developed in Project Whirlwind at MIT. They have been further developed and made commercially available by the Burroughs Adding Machine Co. The ten types of unitized circuits include generators for half-sine-wave pulses of 0.1 microsecond duration, a flip-flop which can be triggered by the pulses and gives out d-c levels for gating, detectors of coincidence between a pulse and a d-c level or between up to five sources of d-c levels, pulse delays, pulse mixers, and channel selectors. Each unit occupies $3\frac{1}{2}$ inches of height in a 19 inch relay rack. They may be interconnected by 93 ohm coaxial cable into complex systems. For example, the Burroughs Laboratory Computer incorporates nearly 500 of these basic pulse control units.

R. D. ELBOURN

NBSEC

1020. H. KOPPEL, "Digital computer plays NIM," *Electronics*, v. 25, Nov. 1952, p. 155–157.

Four stacks of seven chips each are indicated by lights. A "safe" starting condition makes it possible for the player to beat the machine, but not by simply memorizing plays. No electrical diagram appears, but a block diagram shows adders, binary counters, gates, pulser, and scanner. Other

binary game machines at University of Toronto, NBS Corona Labs, etc., are noted. The win theory of this game is given by BOUTON.[1]

J. HOWARD WRIGHT

NBSEC

[1] C. L. BOUTON, "Nim, a game with a complete mathematical theory," *Annals of Math.*, s. 2, v. 3, p. 35–39.

1021. F. C. MULLANEY, "Design features of the Era 1101 Computer," *Electrical Engineering*, Nov. 1952, p. 1015–1018.

The article gives a brief description of a computer using a magnetic drum memory. The first part deals with the basic facts of the machine: what it consists of, what it does, and how it does it. The second part is devoted to the constructional features of the machine and is provided with illustrations. The third section treats the problem of testing and maintenance. Finally, the operational record for over 7000 hrs. is given and a resume of desirable features of this computer presented.

A. WEINBERGER

NBSEC

1022. OFFICE OF NAVAL RESEARCH, *Digital Computer Newsletter*, v. 4, no. 4, Oct. 1952, 11 pages.

The present status of the following digital computers is treated briefly in this number:

1. Naval Proving Ground Calculators
2. The UNIVAC
3. Whirlwind I
4. Computer Research Corporation Computers
   - CADAC 102-A
   - CRC 105
   - CRC 107
5. Moore School Automatic Computer (MSAC)
6. Raytheon Automatic Computer (RAYDAC)
7. The SWAC
8. Aberdeen Proving Ground Computers
   - The ORDVAC
   - The EDVAC
   - The ENIAC
   - The Bell
   - IBM
9. C.S.I.R.O. Mark I

Under Data Processing and Conversion Equipment:

1. Graph Plotter

1023. L. PACKER & W. J. WRAY, JR., "Germanium photodiodes read computer tapes," *Electronics*, v. 25, Nov. 1952, p. 150–151.

A six-channel device for reading paper tape similar to the teletype device uses germanium photoelectric sensing at a speed of 100 pulses per second, although the electronic circuits are capable of 35,000 per second. Small size and large output of the germanium units are advantageous. Only six

diodes are used, but nonetheless this reviewer suggests that reliability is doubtful on the basis of various reports of instabilities due to the plastic encapsulation of these particular diodes.

J. HOWARD WRIGHT

NBSEC

1024. J. RABINOW, "The notched-disk memory," *Electrical Engineering*, v. 71, 1952, p. 745–749.

One of the increasingly pressing problems of government and business is that of the compact storage of large amounts of information in a quickly accessible form.

This paper describes a storage device consisting of many thin iron oxide coated aluminum disks. Information may be recorded on both sides of the disks as coded magnetic pulses. The disks are arranged in the form of a toroid. When it is desired to read or record information on a particular disk, the magnetic recording heads are automatically swung to the chosen disk and the disk is rotated between the recording heads for one revolution.

It is estimated that such a device consisting of 588 disks 20 inches in diameter would have a capacity of a quarter of a billion binary digits. Test results demonstrate that stored data can be reached in times of the order of half a second.

E. F. AINSWORTH

NBSEC

NEWS

Joint Computer Conference.—On December 10–12, 1952, a second joint annual computer conference and exhibition was held in New York under the auspices of the American Institute of Electrical Engineers, Institute of Radio Engineers, and Association for Computing Machinery. The program for the meeting was as follows:

Wednesday, December 10, 1952	Registration and Exhibits
Morning session	S. B. WILLIAMS, *Chairman*, Burroughs Adding Machine Co., Consultant
Keynote address	N. H. TAYLOR, MIT
Recording techniques for digital coded data	A. W. TYLER, Eastman Kodak Co.
Afternoon session	M. M. ASTRAHAN, IBM, *Chairman*
Converters for teletype tape to IBM cards	G. F. NIELSEN, IBM
Punched card to magnetic tape converter for UNIVAC	E. BLUMENTHAL and F. LOPEY, Eckert-Mauchly Div., Remington Rand, Inc.
Devices for transporting the recording media	R. L. SNYDER, JR., Consulting Engineer
Buffering between input-output and the computer	A. L. LEINER, NBS
Thursday, December 11, 1952	
Morning session	W. S. MACWILLIAMS, *Chairman*, BTL
SEAC input-output system:	
SEAC input-output system	S. GRUNWALD, NBS
Input-output devices used with SEAC	J. L. PIKE
Auxiliary equipment to SEAC input-output	RUTH C. HAUETER, NBS
Operating experience	E. AINSWORTH, NBS

UNIVAC input-output system:	
The Uniservo-tape reader and recorder	H. F. WELSH and H. LUKOFF, Eckert-Mauchly Div., Remington Rand, Inc.
Input devices	L. D. WILSON and E. ROGGENSTEIN, Eckert-Mauchly Div., Remington Rand, Inc.
Output devices	E. MASTERSON and L. D. WILSON, Eckert-Mauchly Div., Remington Rand, Inc.
Afternoon session	J. H. HOWARD, *Chairman*, Burroughs Adding Machine Co.
RAYDAC input-output system:	
RAYDAC input-output systems	W. GRAY and K. RAHLER, Raytheon
System design	L. FERN, Raytheon
Operating experience with RAYDAC	F. DEAN, Raytheon
IBM 701 input-output system:	
Type 701 input-output organization	L. D. STEVENS, IBM
Type 726 magnetic tape reader and recorder	W. S. BUSLIK, IBM
Magnetic tape techniques and performance	H. W. NORDYKE, IBM
Friday, December 12, 1952	
Morning session	J. C. MCPHERSON, *Chairman*, IBM
Survey of analog-to-digital data converters	H. E. BURKE, Consolidated Engineering Corp.
Survey of mechanical type printers	J. HOSKEN, A. D. Little, Inc.
Survey of nonmechanical type printers	Lt. R. J. ROSSHEIM, GWU
Anelex printer	L. ROSEN, Anderson-Nichols Co.
Eastman printer	R. G. THOMPSON, Eastman Kodak Co.
Afternoon session	J. G. BRAINERD, *Chairman*, Moore School of Electrical Engineering, Univ. of Penn.
Ferranti input-output equipment	B. W. POLLARD, Ferranti Ltd., London
Garment tag equipment	O. G. HESSLER, Sears Roebuck and Co.
Numerically controlled machine tool	W. PEASE, MIT
Summary and forecast	S. N. ALEXANDER, NBS
Informal discussion	

OTHER AIDS TO COMPUTATION

BIBLIOGRAPHY Z

1025. LEONILDA ALTMAN, "An analog computer as an aid to shower theory calculations," *Rev. Sci. Instruments*, v. 23, 1952, p. 382.

A. c. resolvers are used to solve certain trigonometrical equations.

F. J. M.

1026. S. BOSWORTH, "A new analog computer," *Electronics*, v. 24, no. 8, Aug. 1951, p. 216–224.

This article describes "an inexpensive desk-size electronic differential analyzer" suitable for differential equations with constant coefficients. The device contains 20 d.c. amplifiers, 23 ten-turn potentiometers, and 8 integrating capacitors. The problem is set up on terminal boards which are plugged into the device.

F. J. M.